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High input impedance voltage-mode universal filter and its modification as quadrature oscillator using VDDDAs

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The second order universal voltage-mode filter using voltage differencing differential difference amplifiers (VDDDAs) has been proposed. It has high input impedance voltage-mode biquad filter with orthogonal tune of natural frequency and quality factor. The proposed filter simultaneously provides five filter responses: low-pass (*LP*), high-pass (*HP*), band-reject (*BR*), all-pass (*AP*) and band-pass (*BP*) in the same circuit topology. The natural frequency and quality factor can be tuned electronically and orthogonally dc bias current. The output impedance at output nodes *HP*, *AP* and *BR* has low impedance which can connect to other circuit without the use of voltage buffers. The proposed filter consists of three VDDDAs, one grounded resistor and two grounded capacitors. This makes the proposed filter suitable for integrated circuit development. With slightly modifying the proposed filter, the voltage-mode qudrature sinusoidal oscillator with low output impedance and independent control of condition of oscillation (CO) and frequency of oscillation (FO) has been achieved. The results shown in this paper are from PSPICE simulation and experiment to validate the proposed circuits.

Keywords: Analog filter, VDDDA, Voltage-mode, Single input-multiple output, Oscillator

1 Introduction

The oscillator circuit and analog active filter are popular and standard topic for circuit design. They are widely used for their important requirements for application in electrical and electronic system and also very popular in using for circuit design of continuous-time analog signal processing. There are many fields that using filters circuit such as communications, measurement, and instrumentation, and control systems[1]. Especially, researchers have been very considerably interest in several functions filter which is called universal filter or multifunction filter. The single-input multiple-output (SIMO) is the most popular analog filter where different output filter functions can be simultaneously realized by the same circuit topology[2].

Using of active building block for circuit design is very popular in use. It gives the flexibility for designer to realize the high performance circuit using minimum number of active element[3-7]. With mentioned features, the principle of active building blocks for both current and voltage mode circuit are introduced by Biolek *et al.*[6] Voltage differencing differential difference amplifier (VDDDA)[8] is one of the interests. It allows interesting utilization and design of more profitable or more exacting application especially the electronic controllability. From literature reviews, it is found that not much research using VDDDA has been published for instance the voltage-mode first order all pass filter[8], oscillator[8-10]. The excellent multiple-input multiple-output (MIMO) voltage-mode universal filter using VDDDA was proposed in literature[10-14]. These filters can provide complete standard transfer functions with

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high inputs and low outputs impedance. The natural frequency and quality factor can be electronically and orthogonally controlled. However, these filters cannot be considered as universal filter because all five filter responses cannot be simultaneously provided. The multiple-input single-output (MISO) voltage mode filter was introduced by Herencsar *et al.*[15] This filter consists of single active building block, single MOS transistor and two floating capacitors. It can provide five filter responses depending on the appropriate selecting input voltage. The natural frequency and quality factor can be electronically tuned. However, this filter cannot be easy to cascade without the use of voltage buffers. Moreover, the use of floating capacitors is not attractive for integration.

This contribution presents a SIMO voltage-mode filter with high input impedance, emphasizing on use of VDDDAs. The proposed filter composes of three active elements, one grounded resistor and two grounded capacitors which are suitable for fabricating in monolithic chip or off-the-shelf implementation. The proposed filter can provide five standard functions such as low-pass, high-pass, band-reject, all-pass and band-pass. The quality factor and natural frequency can be electronically and orthogonally adjusted. With slight modification of the proposed filter, the voltage-mode quadrature oscillator with low output impedance is achieved.

2 Principle of Operation

2.1 VDDDA overview

The principle of VDDDA was introduced by Biolek *et al.*[6] Later, Herencsar *et al.*[8] proposed the internal construction of VDDDA using CMOS technology. Symbol and equivalent circuit of VDDDA are shown in Fig. 1 (a) and (b), respectively, where V_+ and V_- are the voltage input terminals which will be converted to be the current at *z* terminal by transconductance (g_m). It is generally tuned by bias current and the differential voltage at terminal *z*, *n* and *p* will be send to *w* terminal with the unity voltage gain. For ideal VDDDA, it has low output impedance at *w* terminal and high input impedance at terminals

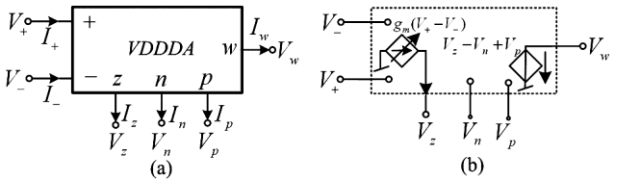

Fig. 1 — VDDDA (a) symbol and (b) equivalent circuit

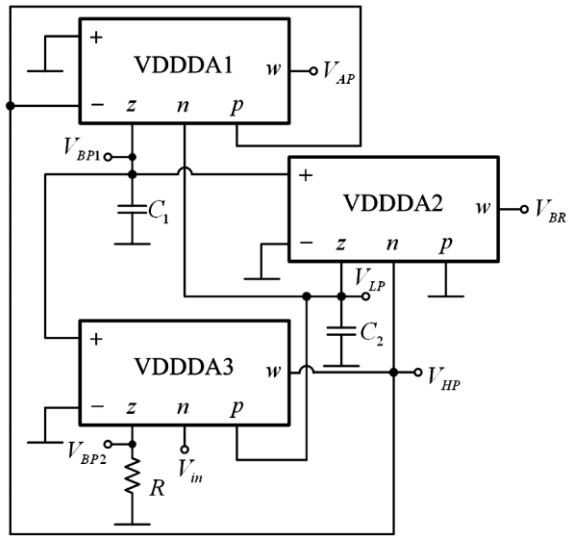

Fig. 2 – Presented voltage-mode filter

V_+, V_-, *z*, *n* and *p*. The characteristics matrix equation of ideal VDDDA is described below:

$$\begin{pmatrix} I_{v+} \\ I_{v-} \\ I_z \\ I_n \\ I_p \\ V_w \end{pmatrix} = \begin{pmatrix} 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ g_m & -g_m & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & -1 & 1 & 0 \end{pmatrix} \begin{pmatrix} V_+ \\ V_- \\ V_z \\ V_n \\ V_p \\ I_w \end{pmatrix} \quad \ldots (1)$$

2.2 High input impedance voltage-mode filter using VDDDAs

Figure 2 is the proposed second order filter consisted of three VDDDAs, one grounded resistor and two grounded capacitors. The proposed filter provides simultaneously five filter responses; *HP*, *LP*, *BR*, *AP* and *BP* (BP_1 and BP_2) with high input impedance. Moreover, the output nodes for *HP*, *AP* and *BR* responses exhibit low output impedance. Considering an ideal VDDDA, routine analysis of the proposed filter provides the following voltage transfer functions:

$$HP(s) = \frac{V_{HP}}{V_{in}} = -\frac{s^2}{D(s)} \quad \ldots (2)$$

$$LP(s) = \frac{V_{LP}}{V_{in}} = \frac{\frac{g_{m1}g_{m2}}{C_1C_2}}{D(s)} \quad \ldots (3)$$

$$BR(s) = \frac{V_{BR}}{V_{in}} = \frac{s^2 + \frac{g_{m1}g_{m2}}{C_1C_2}}{D(s)} \quad \ldots (4)$$

$$AP(s)=\frac{V_{AP}}{V_{in}}=\frac{-\left(s^2-\frac{g_{m1}}{C_1}s+\frac{g_{m1}g_{m2}}{C_1C_2}\right)}{D(s)} \quad \ldots (5)$$

$$BP_1(s)=\frac{V_{BP1}}{V_{in}}=\frac{\frac{g_{m1}}{C_1}s}{D(s)} \quad \ldots (6)$$

$$BP_2(s)=\frac{V_{BP2}}{V_{in}}=\frac{\frac{g_{m1}g_{m3}R}{C_1}s}{D(s)} \quad \ldots (7)$$

where

$$D(s)=s^2+\frac{g_{m1}g_{m3}R}{C_1}s+\frac{g_{m1}g_{m2}}{C_1C_2} \quad \ldots (8)$$

It is found from Eqs (2-8) that the proposed filter is the unit gain filter, then, for any practical use, additional voltage amplifiers are needed to achieve gain from the active filter. However, the gain is probably obtained for BP_1 only if specific quality factor (Q) is set. The natural frequency (ω_0) and Q of each filter response can be expressed as following:

$$\omega_0=\sqrt{\frac{g_{m1}g_{m2}}{C_1C_2}} \text{ and } Q=\frac{1}{g_{m3}R}\sqrt{\frac{C_1g_{m2}}{C_2g_{m1}}} \quad \ldots(9)$$

From Eq. (9), it is found that the quality factor can be electronically tuned via g_{m3} without affecting the natural frequency. Moreover, if g_{m1} is equal to g_{m2}, the natural frequency can be electronically adjusted without affecting the quality factor. However, it is found that the proposed circuit needs component matching conditions (i.e., $g_{m3}=1/R$) for realizing *AP* response. The relative sensitivities of the proposed filter can be found in Eq. (10):

$$\begin{aligned} &S_{g_{m1}}^{\omega_0}=S_{g_{m2}}^{\omega_0}=\frac{1}{2};\ S_{C_1}^{\omega_0}=S_{C_2}^{\omega_0}=-\frac{1}{2};\\ &S_R^{Q_0}=S_{g_{m3}}^{Q_0}=-1;S_{C_1}^{Q_0}=S_{g_{m2}}^{Q_0}=\frac{1}{2};\ S_{C_2}^{Q_0}=S_{g_{m1}}^{Q_0}=-\frac{1}{2} \end{aligned} \quad \ldots(10)$$

It is found that the active and passive sensitivities are equal or less than unity in magnitude.

3 Non-Ideal Case

Practically, the performances of the proposed filter are affected by the influences of voltage tracking error from the unity-value gain of internal differential voltage buffer and parasitic terminal impedances of VDDDA[8]. In this section, these parameters will be taken into account. For non-ideal case the voltage at w terminal is rewritten as shown below:

$$V_w=\beta_zV_z-\beta_nV_n+\beta_pV_p \quad \ldots (11)$$

From Eq. (10), β_z, β_n, and β_p^- are the voltage error gains from z, n, p terminals to w terminal, respectively. The influences of parasitic impedances of V_{-1}, p_1, n_2 and n_3 terminals will be negligible because of their connection to low-impedance outputs (w_3 terminal) and input voltage source. The most importance parasitic impedances are the impedance at z_1 ($R_{z1}//C_{z1}$), n_1 ($R_{n1}//C_{n1}$), V_{+2} ($R_{V+2}//C_{V+2}$), z_2 ($R_{z2}//C_{z2}$) and p_3 ($R_{p3}//C_{p3}$) terminals. However, the parasitic impedances at z_3 terminal will be negligible but the operation frequency f_{op} should be more lower than $1/\{C_{z3}(R_{z3}+R)\}$. The voltage transfer functions for the circuit of Fig. 3 are given in Eqs (12-17):

$$\frac{V_{HP}^*}{V_{in}}=\frac{-\beta_{n3}\left[s^2C_1^*C_2^*+s\left(C_1^*G_2^*+C_2^*G_1^*\right)+G_1^*G_2^*\right]}{D^*(s)} \quad \ldots (12)$$

$$\frac{V_{LP}^*}{V_{in}}=\frac{\frac{\beta_{n3}g_{m1}g_{m2}}{C_1^*C_2^*}}{D^*(s)} \quad \ldots (13)$$

$$V_{BR}^*=\frac{\beta_{n2}\beta_{n3}\left[s^2C_1^*C_2^*+s\left(C_1^*G_2^*+C_2^*G_1^*\right)+G_1^*G_2^*\right]+\frac{\beta_{z2}\beta_{n3}g_{m1}g_{m2}}{C_1^*C_2^*}}{D^*(s)} \quad \ldots (14)$$

$$\frac{V_{BP1}^*}{V_{in}}=\frac{\beta_{n3}g_{m1}\left(s\frac{1}{C_1^*}+\frac{G_2^*}{C_1^*C_2^*}\right)}{D^*(s)} \quad \ldots (15)$$

$$\frac{V_{BP2}^*}{V_{in}}=\frac{\beta_{n3}g_{m1}g_{m3}R\left(s\frac{1}{C_1^*}+\frac{G_2^*}{C_1^*C_2^*}\right)}{D^*(s)} \quad \ldots (16)$$

$$V_{AP}^*=\frac{-\left\{\begin{array}{l}\beta_{n3}\left[s^2C_1^*C_2^*+s\left(C_1^*G_2^*+C_2^*G_1^*\right)+G_1^*G_2^*\right]-\\ \beta_{z1}\beta_{n3}g_{m1}\left(s\frac{1}{C_1^*}+\frac{G_2^*}{C_1^*C_2^*}\right)+\frac{\beta_{n3}g_{m1}g_{m2}}{C_1^*C_2^*}\end{array}\right\}}{D^*(s)} \quad \ldots (17)$$

where

$$D^*(s)=\left[\begin{array}{l}s^2+s\left(\frac{G_2^*}{C_2^*}+\frac{G_1^*}{C_1^*}+\frac{\beta_{z3}g_{m1}g_{m3}R}{C_1^*}\right)+\\ \frac{G_1^*G_2^*+\beta_{z3}g_{m1}g_{m3}RG_2^*+\beta_{p3}g_{m1}g_{m2}}{C_1^*C_2^*}\end{array}\right] \quad \ldots (18)$$

$C_1^* = C_1+C_{z1}+C_{v+2}+C_{v+3}$, $C_2^* = C_2+C_{z2}+C_{n1}+C_{p3}$, $G_1^* = G_{z1}+G_{v+2}+G_{v+3}$ and $G_2^* = G_{z2}+G_{n1}+G_{p3}$. Also non-ideal values of ω_0 and Q are found in Eqs (19) and (20), respectively:

$$\omega_0^* = \sqrt{\frac{G_1^*G_2^* + \beta_{z3}g_{m1}g_{m3}RG_2^* + \beta_{p3}g_{m1}g_{m2}}{C_1^*C_2^*}} \quad \ldots (19)$$

$$Q^* = \frac{1}{\left(\begin{matrix}C_1^*G_2^* + C_2^*G_1^* + \\ \beta_{z3}C_2^*g_{m1}g_{m3}R\end{matrix}\right)}\sqrt{C_1^*C_2^*\left(\begin{matrix}G_1^*G_2^* + \beta_{z3}g_{m1}g_{m3}RG_2^* + \\ \beta_{p3}g_{m1}g_{m2}\end{matrix}\right)} \quad \ldots (20)$$

4 Simulations Results

PSPICE simulations of the proposed filter in Fig. 2 were performed. The implementation of the CMOS VDDDA was same as described elsewhere[8]. Parameters of a 0.18 µm TSMC CMO Stechnology[16] (level 7) with ±0.9 V voltage supply and V_B = -0.35 V was used for simulation of PMOS and NMOS transistors. From Table 1, aspect ratios of PMOS and NMOS transistor are listed. It is seen that the parasitic resistances at terminals V_+, V_-, n, and p (R_{v+}, R_{v-}, R_n and R_p) exhibit high because they are gate resistance. Other simulated parasitic element values for each terminal (I_B = 50 µA) are C_{v+} = 55.5 fF, C_{v-} = 53.2 fF, R_z = 570.54 kΩ, C_z = 15.4 fF, C_n = 4.24 fF and C_p = 4.25 fF. The simulated voltage error gains, β_z, β_n, and β_p are equal to 0.997. The filter was designed with the parameters of its components as follows: $C_1 = C_2 = 47$ pF, R = 3.3 kΩ, $I_{B1} = I_{B2} = I_{B3}$ = 50 µA. It yields the natural frequency of 1.047 MHz and quality factor of 1. The theoretical pole frequency is about 1.058 MHz. From the results, the gains responses for *LP*, BP_1, BP_2 and *HP* of the proposed filter obtained from Fig. 2 are shown in Figs 3-5 which are the gain response and phase response of *BR* and *AP* responses, respectively. It is obviously that the proposed filter can simultaneously provide low-pass, high-pass, band-pass, band-reject and all-pass functions without modifying circuit topology. The gain response of BP_2 difference I_{B3} is shown in Fig. 6, where I_{B3} was set to 20 µA, 50 µA and 200 µA. The quality factor evaluated based on the simulation results was 1.49, 1, and 0.65, respectively. This is confirmed by Eq. (9) that the quality factor can be electronically tuned by I_{B3} without affecting the natural frequency. High Q value can be achieved by setting I_{B3} as low as possible. The highest simulated Q is 26.66 (I_{B3} = 1 µA) and the lowest simulated Q is 0.384 (I_{B3} = 400 µA).

Table 1 – Dimensions of the transistors

Transistor	W (µm)	L (µm)
M1-M2, NMOS (AGC)	9	1.08
M3-M4	3.96	1.08
M5-M7	3.6	1.8
M8-M11	0.72	1.08
M12-M14	2.16	1.08

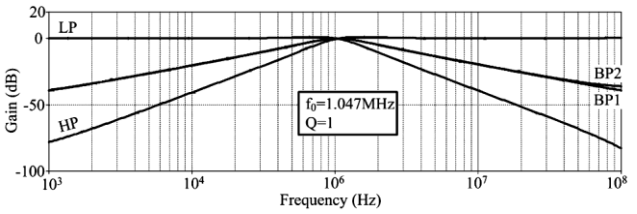

Fig. 3 – Frequency responses of proposed filter *LP*, BP_1, BP_2 and *HP*

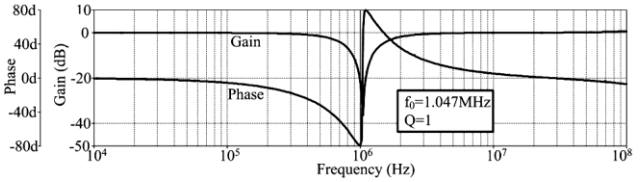

Fig. 4 – Gain and phase response of *BR*

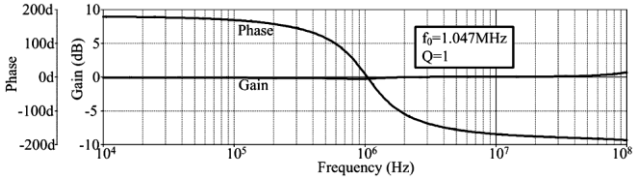

Fig. 5 – Gain and phase response of *AP*

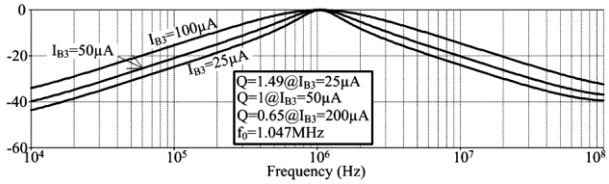

Fig. 6 – BP_2 responses for difference I_{B3}

Figure 7 shows the dependence of the THD of LP filter on input voltage level. The THD is not over 1% when the input signal is lower 650 mV. In this test, sinusoidal signal with 100 kHz in-band frequency was fed into the proposed filter.

5 Comparison with Existing SIMO Voltage-Mode Filters

The proposed SIMO voltage-mode filter in Fig. 2 is compared with several SIMO voltage-mode filters from[17-44]. It is found from Table 2 that there are VM

MISO structures having even some low-output impedance outputs[25,29,32,38,42]. However, their other drawbacks are in missing possibility for electronic control, requirements for floating passive elements and higher number of active elements (4 or 5). All these problems are solved in solution presented in this paper.

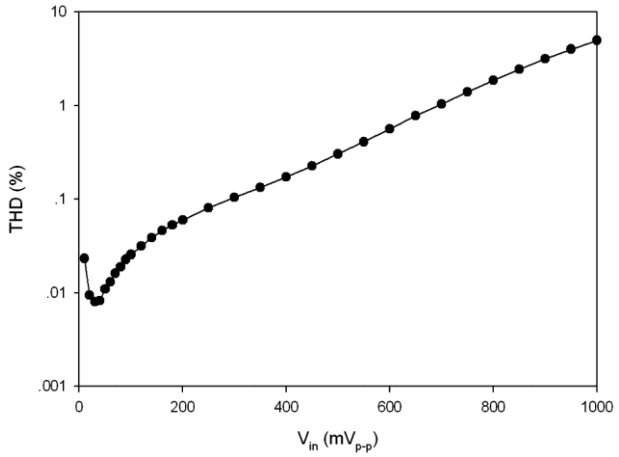

Fig. 7 – Dependence of output harmonic distortion of *LP* filter on the input voltage

6 Modification of Proposed Filter as Quadrature Oscillator

By connecting node V_{BP1} to V_{in} and interconnecting terminal V_+ and V_- of VDDDA1 and VDDDA2 of the circuit in Fig. 2 according to the principle reported in earlier study[45] as illustrated in Fig. 8, the voltage-mode quadrature oscillator with low output impedance can be achieved. The characteristic equation of the oscillator in Fig. 8 is obtained as:

$$s^2 + (1 - g_{m3}R)\frac{g_{m1}}{C_1}s + \frac{g_{m1}g_{m2}}{C_1C_2} = 0 \quad \ldots (21)$$

According to Eq. (21), the frequency of oscillator (FO) and condition of oscillation (CO) is written as:

$$\omega_0 = \sqrt{\frac{g_{m1}g_{m2}}{C_1C_2}}, \text{ and } 1 \le g_{m3}R \quad \ldots (22)$$

Table 2 – Comparison of various SIMO voltage-mode filters

Reference	ABB	No. of ABB	No. of *R*+*C*	Grounded elements only	High input impedance	Electronic tune	Orthogonal tune of *Q* and ω_0	Five filter responses	Low output impedances	Technology
17	DVCC	3	3+2	yes	yes	no	no	yes	no	CMOS
18	DVCC	3	3+2	no	yes	no	yes	yes	no	CMOS
19	DVCC	2	3+2	no	no	no	yes	yes	no	CMOS
20	FDCCII (Fig. 3)	1	2+2	yes	yes	no	no	no	no	CMOS
21	DDCC	2	3+2	no	no	no	no	yes	no	CMOS
22	DDCC	3	2+2	no	no	no	no	yes	no	CMOS
23	DDCC & OTA	2	1+2	yes	yes	yes	no	no	no	CMOS
24	OTA	8	0+2	yes	yes	yes	yes	no	no	CMOS
25	CFOA	1	3+2	no	no	no	yes	no	LP	commercial IC
26	DDCCTA	1	1+2	yes	yes	yes	no	no	no	CMOS
27	DDCCTA	2	2+2	yes	yes	yes	no	yes	no	CMOS
28	OTA	8	0+2	yes	yes	yes	yes	no	no	CMOS
29	DDCCTA	3	0+2	yes	yes	yes	no	yes	AP	CMOS
30	CCCCTA	1	1+3	no	no	yes	yes	no	no	BJT
31	DDCCTA	1	2+2	no	no	yes	no	no	no	CMOS
32	DDCCTA	2	2+2	yes	yes	yes	no	yes	AP	CMOS
33	FDCCII	1	3+2	no	no	no	no	yes	no	CMOS
34	DVCC	4	5+2	yes	yes	no	yes	no	no	CMOS
35	ICCII	2	4+2	no	no	no	no	no	no	CMOS
36	DVCC	2	2+3	no	no	no	no	no	no	CMOS
37	DDCCTA	2	2+2	no	yes	yes	yes	yes	no	CMOS
38	VD-DIBA	2	0+2	yes	yes	yes	no	no	HP	commercial IC
39	VDCC (Fig. 3)	1	2+2	yes	no	yes	yes	no	no	CMOS
40	VDCC	1	2+2	no	no	yes	yes	no	no	BJT
41	CCII	2	3+2	no	yes	no	no	no	no	CMOS
42	DDCCTA	2	3+2	yes	yes	yes	yes	yes	AP	CMOS
43	VDTA (Fig. 5)	1	0+2	yes	yes	yes	no	no	no	CMOS
44	CCII	4	5+2	no	yes	no	yes	yes	no	commercial IC
Present work	VDDDA	3	1+2	yes	yes	yes	yes	yes	HP, AP, BR	CMOS & commercial IC

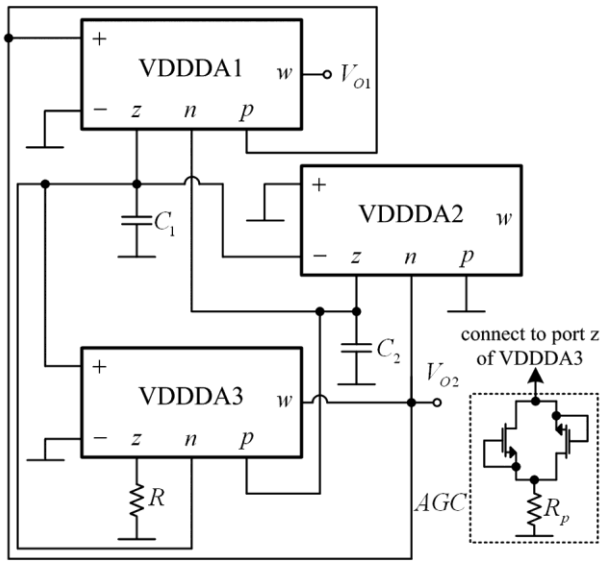

Fig. 8 – Voltage-mode quadrature oscillator with low output impedance

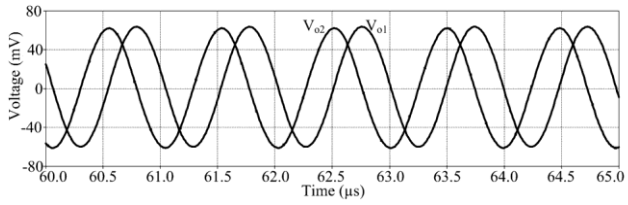

Fig. 9 – Quadrature output waveform

It is found from Eq. (22) that the FO and CO are independently and electronically controlled. The relationship of V_{O2} and V_{O1} is follows:

$$\frac{V_{O2}}{V_{O1}} = \frac{sC_1}{g_{m1}g_{m3}} \quad \ldots (23)$$

At oscillation frequency (ω_0), the magnitude of V_{O2}/V_{O1} is written as:

$$\left|\frac{V_{O2}}{V_{O1}}\right|_{\omega_0} = \frac{1}{g_{m3}}\sqrt{\frac{C_1 g_{m2}}{C_2 g_{m1}}} \quad \ldots (24)$$

It is found from Eq. (24) that the changing of g_{m1} or g_{m2} for controlling the FO causes change of amplitude V_{O2} and V_{O1} during tuning process. This phenomenon will increase the THD if amplitude reaches high levels due to the limits of dynamical range of VDDDA. However, this can be alleviated by simultaneously changing g_{m1} and g_{m2} ($I_{B1} = I_{B2}$). As stated above, the amplitude of quadrature output

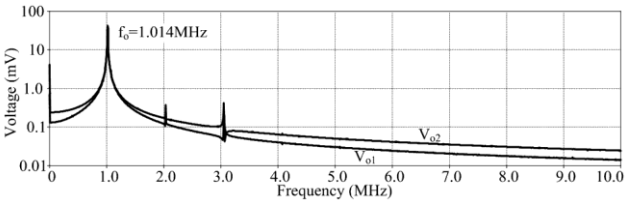

Fig. 10 – Output spectrum

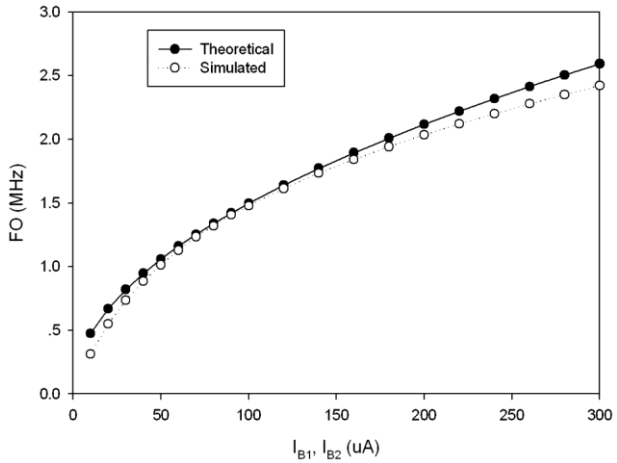

Fig. 11 – Tuning of FO by adjusting I_{B1} and I_{B2}

voltage V_{O1} and V_{O2} is equal for all frequency. However, to unify unbalance of produced amplitudes V_{O1} and V_{O2} as well as to reduce the THD, the simple AGC circuit for amplitude stabilization can be easily applied to terminal *z* of VDDDA3.

The proposed oscillator in Fig. 8 was simulated with the parameters of its components; $C_1 = C_2 = 47$ pF, R = 3.3 kΩ, R_p = 330 kΩ, $I_{B1} = I_{B2} = 50$ µA and $I_{B3} = 51.5$ µA. The W/L of NMOS in AGC is 9 µs /1.08 µm. It yields the FO of 1.014 MHz. The theoretical FO is about 1.058 MHz. The results of this simulation are, respectively, shown in Figs 9 and 10. The total harmonic distortion for V_{O1} and V_{O2} are 0.68 % and 76 %, respectively. Tuning of simulated and theoretical FO is shown in Fig. 11, where I_{B1} and I_{B2} are equal and were adjusted from 10 µA – 300 µA. The range of FO controlled from 0.31 MHz –2.42 MHz was obtained. It is found that there is some deviation between theoretical and simulated value due to the parasitic element as analyzed in Eq. (19). The tuning of g_m by adjusting I_B will change the value of parasitic elements.

7 Experimental Results

The performances of the proposed filter and oscillator were also experimentally investigated. The

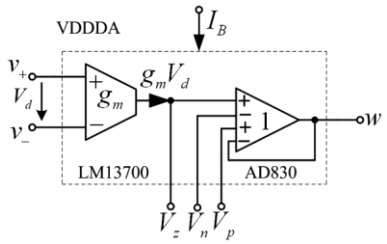

Fig. 12 – Internal construction of VDDDA constructed from an available commercial ICs

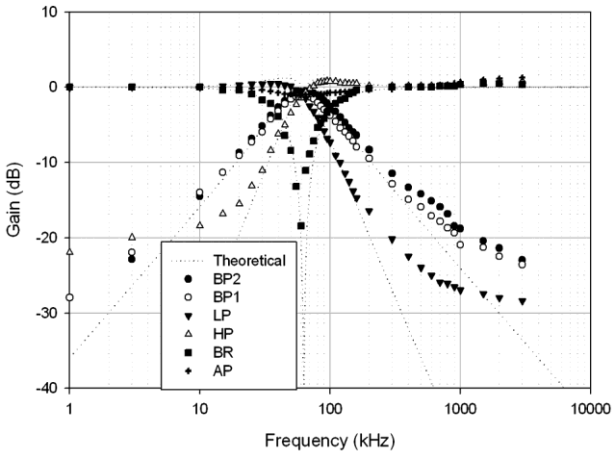

Fig. 13 – Experimental gain responses of the proposed filter

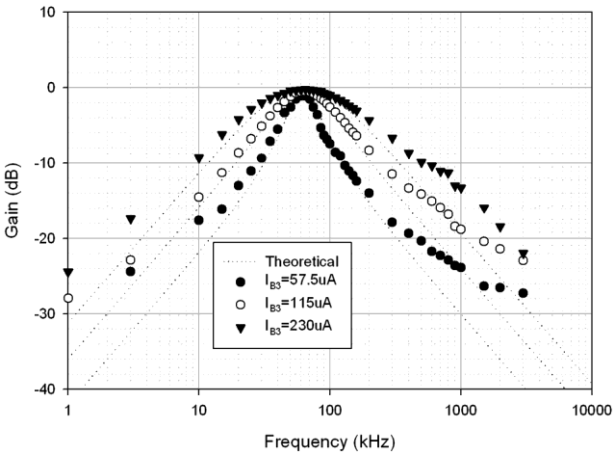

Fig. 14 – Experimental gain response of BP_2 for different value of I_{B3}

VDDDA was constructed from the available commercial ICs, AD830 and LM13700 as illustrated in Fig. 12. The transconductance of LM13700 is $g_m = I_B / 2V_T$ where V_T is thermal voltage ($V_T \cong 26$ mV at room temperature). The proposed filter was firstly tested with following conditions; the supply voltage ±5 V, $C_1 = C_2 = 5.6$ nF, $I_{B1} = I_{B2} = I_{B3} = 115$ µA

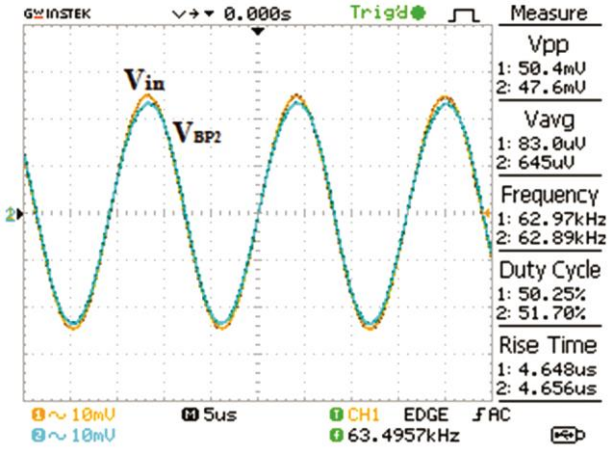

Fig. 15 – Measurement of V_{BP2} at frequency 63 kHz

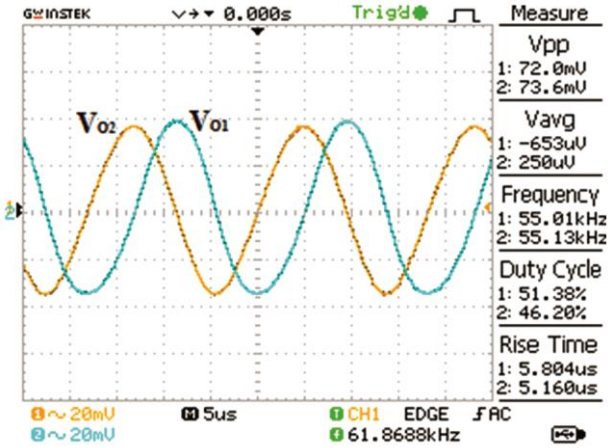

Fig. 16 – Measurement of output voltage and its spectrum where $I_{B1} = I_{B2} = 115$ µA

($g_{m1} = g_{m2} = g_{m3} = 2.211$ mA/V) and $R = 0.45$ kΩ. With these conditions, the natural frequency and quality factor are 62.853 kHz and 1, respectively. The experimental gain response of BP_2, BP_1, LP, HP, BR and AP is shown in Fig. 13. The experimental natural frequency is about 61 kHz which was about 2.948 % deviated from theoretical value. The tuning of Q without affecting natural frequency is confirmed by the experimental result of BP_2 filter in Fig. 14 where the value of I_{B3} was changed to 57.5 µA, 115 µA and 230 µA. The measurements of output voltage V_{BP2} is also shown in Fig. 15 where the 50 mV sinusoidal voltage with 63 kHz of frequency was applied as input signal.

The proposed oscillator in Fig. 8 was tested with following conditions; the supply voltage ±5 V, $C_1 = C_2 = 5.6$ nF, $I_{B1} = I_{B2} = I_{B3} = 115$ µA ($g_{m1} = g_{m2} = g_{m3} = 2.211$ mA/V) and $R = 0.54$ kΩ.

With these conditions, the FO is 62.9 kHz. Figure 16 shows the measured output voltage where the experimental FO was about 61.86 kHz which was about 1.579 % deviated from theoretical value. It is also found that the output voltages V_{o1} and V_{o2} are quadrature sinusoidal signal.

8 Conclusions

Voltage-mode bi-quad filter has been proposed in this study. The advantages of the proposed filter are as follows. Firstly, it can perform variety of filters, i.e., low-pass, high-pass, band-pass, band-reject and all-pass functions. Secondly, the quality factor and the natural frequency can be electronically and orthogonally controlled. Finally, the filter has high input impedance. Moreover, the output voltage terminals for functions high-pass, band-reject and all-pass are low output impedance. The proposed filter consists of three VDDDAs, one grounded resistor and two grounded capacitors, which are attractive for either IC implementation. With slightly modifying the proposed filter, the voltage-mode quadrature oscillator low output impedances is achieved. The CO and FO can be independently and electronically tuned. Moreover, the ratio of amplitudes V_{O1} and V_{O2} is constant on the tuning of FO if I_{B1} and I_{B2} are simultaneously tuned. Simulation results confirmed theoretical anticipation and validity of the synthesis. The power consumption for proposed filter is 0.343 mW and for proposed oscillator (with AGC circuit) is 0.346 mW. Moreover, the experimental results using available commercial ICs (AD830 and LM13700) are included and they meet very well with theoretical presumptions.

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