

Material properties analysis of graphene base transistor (GBT) for VLSI analog circuits design

Gurinder Pal Singh^{a*}, Balwinder Singh Sohi^b & Balwinder Raj^c

^aDepartment of Electronics and Communication, Chandigarh University, Mohali 140 413, India

^bChandigarh University, Mohali 140 413, India

^cNational Institute of Technology, Jalandhar 144 011, India

Received 1 December 2016; accepted 6 May 2017

Graphene base transistor's (GBT) analysis has been reviewed in this paper. This study has been focused on work carried out by other authors for GBT physics. Here prominence has been given to material properties and their effects on GBT for VLSI analog circuit design to operate in high frequency range of THz. Various papers in literature have been reported for the implementation of designs with different emitter and collector materials. Materials properties are the controlling parameters to decide cut-off frequency (f_T), trans-conductance, gain and off current (I_{off}) in GBT. The implemented results of literatures signify that the electron affinity and work function of emitter and collector are the dominant factors for flow of charges from emitter to collector. Dependency of these two parameters on dielectric constant and thickness of emitter-base insulator (EBI) and base collector insulator (BCI) that are tantalum pentoxide (Ta_2O_5), carbon-doped silicon oxide (SiCOH) and SiO_2 has been studied. Effects of collector and BCI thickness have been investigated in detail to scrutinize base leakage current by the virtue of back scattering in collector-BCI interface. Small signal equivalent circuit model for GBT have also been studied by including parasitic capacitance behaviour between graphene Dirac-point potential with respect to graphene fermi level, emitter, EBI, BCI and collector fermi level potential.

Keywords: GBT, BCI, EBI, Work function, Permittivity, Electron affinity

1 Introduction

The performance improvement of existing electronic design and to evolve new devices for better performance, study of new materials is essential. Understanding of device physics contributes toward efficient use of devices at application level. Schrodinger wave equation is used to present material's electronic behaviour for utilizing transistor implementation. Gordon Moore in 1965 set a target for electronic industry for the rate of growth of number of transistor on IC¹. To keep the Moore's law alive, electronics industry is now working in deep submicron region of device modelling. Beyond 16 nm, short channel effects degrade transistor's performance. Up to 7 nm silicon has proved as a reliable semiconductor, fulfilled the expectation of semiconductor industry to reach out designing of ultra large scale integrated transistor design².

Now semiconductor industry is about to enter into new area of designing, where further scaling of silicon is not possible². Reason for the limits of silicon scaling is related to its poor selectivity and generation

of lithographic patterns are not possible for silicon beyond this limit³. There are two solutions for this problem, either to find out materials that can be physically scaled down in nano range and can attain faster switching speeds, or to find out solutions that rely on other than electricity that is light⁴. Prerequisite to work with new materials is to have well established fabrication technologies. While evaluating performance of a material during its implementation for transistor designing, various parameters have to be taken care depending upon targeted application. Some parameters like physical dimensions, on/off current ratio, cut off frequency, intrinsic gain; voltage swing decides the performance characteristics of devices irrespective of the device application. Even usage of Germanium has been also explored but process of growing GeO_2 on Ge surface requires tremendous accuracy and control⁵.

Working in this direction graphene comes out as promising material for improvement of electronics devices operating at higher frequencies. Graphene's 2-D nature is proved a solution to roadblocks of nanotechnology for enhancing circuit performance⁶. Graphene carbon based allotrope offers distinct

*Corresponding author (E-mail: gurinder.pal@cumail.in)

advantages in variety of applications⁷. Researchers are exploring graphene as single sheet, cylindrical tube (carbon nanotube), buckeye ball (quantum dot) as channel in the field effective transistors and interconnects levels also. Using graphene as channel has pushed the limits of complementary metal oxide semiconductor (CMOS) technology^{8,9}.

From literature and reported results of various research papers it has been proved that using graphene nano-ribbon as channel in the field effective transistors leads to large off current with high output conductance⁷. GFET structure is explored largely at various potentials which showed intrinsic cut-off frequency¹⁰ about 400 GHz. It could be possible to make GFET (graphene field effect transistor) work in THz range but its high off current limits its usage in the range of such high cut off range for digital applications⁶. Maintaining band gap to have low or zero off current is not an easy task in case of GFET due to various fabrication issues. The graphene in cylindrical form called CNT (carbon nano tubes), rather than single sheet or ribbons is another prospective which attracts the researchers. CNTFET provides approximately I_{on}/I_{off} is the range¹¹ of 10^6 . But fabrication of carbon nanotube as channel in FET is a challenging job¹². Having best possible device structural arrangement of graphene to solve issue of I_{off} current, related parameters as well as to develop compatible fabrication process with existing silicon technique is the challenging job. In this paper we have discussed the physics of the graphene while using in the heterojunction arrangement with other materials followed by its working. In this heterojunction arrangement graphene is used in vertical for firstly introduced¹³ in 2012. This paper consolidates the material analysis performed by various authors.

2 GBT Device Structure

In GBT device structure graphene single layer is used in vertical arrangement as shown in Fig. 1. Here charge carriers move normal to layer irrespective of GFET where flow of charge carriers is laterally. GBT arrangement is similar to bipolar junction transistor

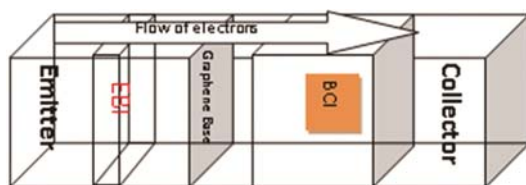


Fig. 1 — GBT structure¹⁴.

(BJT). In vertical arrangement graphene acts as base forming heterojunction on both sides with other materials which is a different scenario from BJT. Graphene has indirect contact to emitter and collector. Two insulator layers are used between emitter and collector of varying thickness as shown in Fig. 1. Thickness of emitter base insulator (EBI) is less comparative to collector base insulator¹⁴. This arrangement is similar to hot electron transistor (HET) first introduced in 1960 and metal-insulator-metal-insulator-metal arrangement¹⁵ introduced in 1986. Optimization of HET was restricted by metal-base resistance, which increases rapidly while scaling down base width¹⁶. To overcome the problem of GFET and HET, graphene is used as base in HET, because of its single atom thickness. GBT utilizes the concept of quantum tunnelling for conduction of device carriers from emitter to base and base to collector. This novel approach helps in achieving almost negligible off current¹⁷. GBT was first proposed in 2012 by Vaziri *et al.*¹⁸. In his work metal was used as a collector and doped silicon as emitter.

2.1 Fabrication steps of GBT

CMOS technology compatible fabrication process is used for the GBT fabrication. Whole fabrication method was divided in four steps.

Step 1: Etching of trenches in Si Substrate

- (i) Filling with high density plasma SiO₂.
- (ii) Chemical mechanical polishing.
- (iii) Emitter development (Phosphorus Implantation).
- (iv) 5 nm SiO₂ EBI grown by thermal Oxidation

Graphene deposition method is as follow¹⁸:

Step 2: Chemical vapour deposited (CVD) graphene then transferred from copper surface¹⁹.

- (i) Transfer Process: PMMA (polymethyl methacrylate) is spin deposited to one side of copper/graphene substrate.
- (ii) Backside of graphene is removed in oxygen plasma.
- (iii) Copper film is selectively etched in FeCl₃.
- (iv) Then rinsing PMMA/Graphene film in deionized water and transferred from solution to Si chips.
- (v) Removal of PMMA: Wet chemical treatment in acetone and chloroform. Followed by annealing process at 350 °C to evaporate residual solvents and polymer.
- (vi) Quality of transferred graphene is confirmed by Raman spectroscopic²⁰.

Step 3: BCI development includes deposition of 3 nm Al seed layer depo-evaporation, followed by its exposure to ambient air to form aluminised by e-beam um Oxide

- (i) To form Al₂O₃: Atomic layer deposition is used with standard trimethyl aluminium/water process.
- (ii) Thickness of Al₂O₃ confirmed by spectroscopic ellipsometry.
- (iii) All measurements are performed at room temperature and ambient air.

Step 4: e-beam evaporation in combination with a lift-off technique used for deposition of base contacts. With this technique, Base contacts of 15 nm Ti/70 nm Au deposited.

2.2 Operation of GBT

Concept behind the working of GBT device is similar to hot electron transistor (HET). Charge from emitter has to tunnel through EBI. Tunnelling behaviour of the charge particle is presented by time dependent schrodinger:

$$\frac{-\hbar^2}{2m} \frac{\partial^2 \Psi(x,t)}{\partial x^2} + U(x)\Psi(x,t) = i\hbar \frac{\partial^2 \Psi(x,t)}{\partial t^2} \quad \dots (1)$$

where, $\Psi(x,t)$ represents wave functions, $U(x)$ is potential energy, \hbar is modified Plank's constant ($6.626176 \times 10^{-34} / 2\pi$ joule-s).

Figure 2 gives the overview for graphene base transistor working based on its band theory. In normal mode of operation when no potential or zero potential (V_{BE}) is applied between base and emitter, conduction band of insulator (EBI) remains flat. As work function (Φ_1) of insulator is very much higher in comparison to semiconductor (Φ_S), silicon in this scenario. Electrons do not have sufficient energy to cross this high-energy barrier. This state is counted as cut-off state, when no current is flowing pointing towards zero off current, which is not achievable in GFET. In this situation potential applied at collector has no effect. When some positive potential is applied at graphene base, holes accumulated in graphene due to finite density of states which forced fermi level below to neutrality point. V_{BE} must be less than V_{CE} . The charge²¹ stored in graphene is given by Q_B as given in Eq. (2):

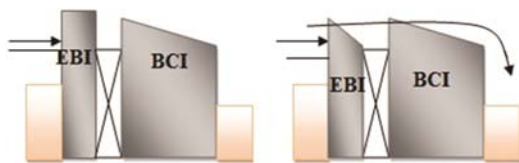


Fig. 2 — GBT band structure in off and on mode of operation¹⁷.

$$Q_B = \int_{-\infty}^{U_B} \frac{(U_B - E) \exp[(E - E_{fb})/KT]}{1 + \exp[(E - E_{fb})/KT]} dE \quad \dots (2)$$

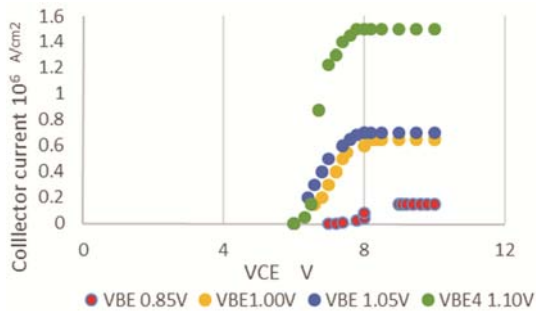
Here U_B represents neutrality point or dirac-point energy, K is Boltzmann constant, E_{fb} is the fermi level in the base and T is temperature.

Applied V_{BE} causes voltage drop which appears across EBI. This voltage drop causes the bending of conduction band for insulator near to base side, as shown in Fig. 2. This band bending is due to capacitive effect. Now electrons from emitter side have sufficient energy that helps to tunnel quantum mechanically from the insulator to base. In prospective of quantum mechanical, tunnelling electron behaves as charge inside the infinite potential well. For having effective tunnelling, applied voltage must be greater than the metal-insulator work function¹⁵. V_{CE} potential between collector and emitter further helps the charge particle to reach at collector section by tunnelling through collector base insulator (BCI). EBI barrier is controlled by V_{BE} and current is function of EBI thickness causing current dependency on V_{BE} . Linear decrease in the thickness will lead to an exponential growth in the tunnelling current. So at fabrication time thickness of EBI must be well controlled. BCI thickness stimulus collector current and base backscattering phenomenon.

3 Performance Analysis of GBT

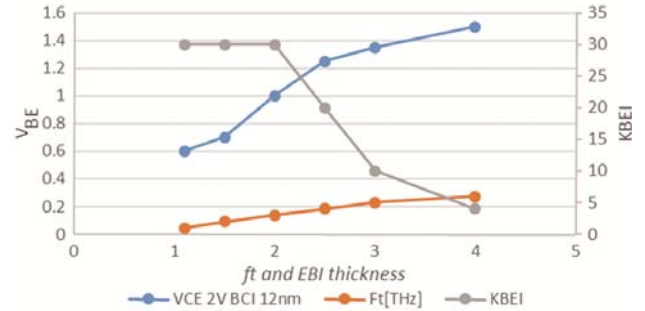
GBT is thinner device relative to other heterojunction devices. Mehr W *et al.*¹³ did the GBT DC analysis. SiO₂ used as BCI and Erbium-germane (Er₂Ge₃) as EBI. Electron affinity for Ge is taken as 4.0 eV with 4.05 eV work function of Er₂Ge₃. BCI can stand V_{BC} up to 10 V. GBT has shown good power performance for these specifications. While using in common emitter configuration, simulations conveyed that for $V_{BE} = 0$ V device remains in off state irrespective of potential is applied between emitter and collector. By rising V_{BE} more than 0 GBT switched on. For very low value of V_{BE} very low collector current is observed. If V_{BE} is minted at 1.10 V and $V_{EC} = 8$ V forced GBT in linear mode operation. As V_{CE} approaches to 10 V, device enters into the saturation mode, and having maximum J_C ¹⁷ shown in Fig. 3.

For high frequency applications, GBT has proved a remarkable device. With BCI thickness of 12 nm, $K=4$ for fix $V_{BC} = 2$ V neutrality point shifts more to upward with increase in EBI thickness²¹. When EBI is fixed at 2 nm, finite density of states (DoS) of graphene tends to reduce its transconductance (g_m).

Fig. 3 — V_{BE} effect on mode of GBT operation.

Cut off frequency (f_T) is also the function of emitter base insulator (EBI). GBT is able to work at terahertz frequencies when EBI thickness varies from 1 nm – 2 nm, with metal emitter work function (Φ) less than or equal to 0.5 eV. For these values of EBI thickness and Φ , very less variations are observed in GBT performance in terahertz range for K varying from 10 to 30. Increase in EBI thickness degrades device g_m and at same time value of K is also large it will lower f_T . GBT is no longer compatible for higher frequency operations²¹. Collector current density (J_C) is another parameter which decides device performance at higher frequency applications. J_C is less affected by variations in V_{CE} relative to V_{BE} . GBT shows maximum performance when Φ approaches to 0.5 eV, $V_{CE} = 2$ V fix and V_{BE} approaches to 1.5 V from 0.6 V with relative permittivity $K=4$. During DC analysis it has been observed that as V_{BE} approaches higher (>1.5 V), collector current density is least affected by the variations in EBI thickness and permittivity (K). For $K=4$ to 10 g/J_C approaches to 2.5 V^{-1} . These results indicate that larger the thickness lower will be the current density. If target is to operate GBT as amplifier for EBI thickness = 1.5 nm and BCI thickness = 12 nm with fix insulator relative permittivity 4, it becomes necessary to have V_{BE} in the range 1 V – 1.5 V for stable gain of device. Too small value of emitter base biasing is not acceptable because these provide lesser and unstable intrinsic voltage gain. All these relation in ft and V_{BE} , V_{CE} , and K is shown in Fig. 4.

Carrying this analysis to the next level Venica *et al.*¹⁴ has performed simulation for various EBI and BCI materials. During simulation emphasises given on impact of relative permittivity of insulators. Here experiment is performed in two phase. In first phase emitter material is changed with respect to various value of permittivity of insulators. In first step of second phase tantalum pentoxide (Ta_2O_5) is preferred

Fig. 4 — Effect of various materials parameters and V_{BE} on ft .

both as EBI and BCI followed by second step which includes carbon-doped silicon oxide (SiCOH) for both the insulating layer. Then combination of Ta_2O_5 and SiCOH as EBI and BCI layer, respectively.

It is observed that GBT performance is very much affected by dielectric constant/relative permittivity of the insulator. While using highly doped ($N_D=10^{19} \text{ cm}^{-3}$) n -type silicon emitter and EBI with $K=30$ then collector current density remains high for all values of V_{BE} . But in case of metal as emitter for achieving higher J_C value of K should be lower, with V_{BE} not exceeding 1.8 V. If K approaches 30, then larger V_{BE} are not accepted, it degrades device performance in terms of collector current density. At same high current effects start appearing if V_{BE} is raised up beyond 1.8 V. Drift velocity (v_d) is also a performance controlling parameter in-terms of transition frequency (f_T), because of direct relation with g_m . By lowering v_d below 10^7 cm/s then GBT will no longer able to operates in tetra hertz region of operation.

Due to variation in work function for metal, semiconductor and insulator selection of the material for emitter, collector and respective insulator turns out a critical job for designers. Larger BCI thickness degrades devices performance in THz region. Because for charges to tunnel from BCI to collector, BCI should have more bending at collector side. That is possible if BCI shows more capacitive effect. But larger thickness (t_{ox2}) results in the less charge. By using BCI material with high value of K , compensate the drawback of BCI thickness as per the relation given in Eq. (3) below:

$$c = K A/d \quad \dots (3)$$

where, K is dielectric constant of insulator material, A is area of capacitor plates (here graphene and Si is acting as capacitor plates), d is distance between plates here t_{ox2} . It is also analysed that while using metal (Ti) instead of Si (n -doped) as emitter and

collector region, low K insulator material becomes essential if thicknesses ($t_{ox1}t_{ox2}$) is chosen to be same for both regions. Insulator with high- K is preferred for Si-emitter based GBT. Work function and electron affinity of the materials are key factors behind selection of dielectric constant for EBI-BCI layer. To have device with better performance with f_T in tetra hertz range it is better to use thin (t_{ox1}) EBI. Vaziri *et al.*¹⁸ in 2013, while using graphene as base of HET transistor instead of metal, used SiO_2 as insulator for EBI layer with t_{ox1} which approaches to 5-8 nm. Tunnel barrier height of this insulator is 3.2 eV with respect to silicon, triggering very low-on current that reduced the performance of GBT. Reduction in t_{ox1} that will lower barrier height would be the solution to enhance tunnelling current. But thinner insulator higher will be the defects. Also, thinner t_{ox1} cannot shield the cold electrons tunnelling. Vaziri *et al.* proposed a solution to this problem by utilizing bilayer insulator^{9,22}. Idea behind this approach was to suppress direct tunnelling (DT) that causes cold electrons to super pass barrier and defect mediated currents. To have better current density for higher frequency device it is necessary that Fowler-Nordheim tunnelling dominates in GBT. In bilayer dielectric arrangement it becomes necessary to have one layer with high quality dielectric as layer-1 and high electron affinity/low band gap dielectric as layer-2 with suitable thickness. A novel dielectric thulium silicate (TmSiO) was used as a first layer 1 nm in thickness. For second layer, experiment was performed with higher electron affinity materials HfO_2 and TiO_2 for varying thickness. In this work five different samples were taken of varying thicknesses, that are Al_2O_3/HfO_2 , $TmSiO/HfO_2$, $TmSiO/Tm_2O_3$, $TmSiO/TiO_2$, $TmSiO$. $TmSiO$ came out as the best insulator to be used as first insulator layer because it forms better interface with silicon emitter. High dielectric constant with lower electron affinity of $TmSiO$ favours usage of this novel insulator material as layer-1 to have step tunnelling. While using Al_2O_3/HfO_2 for EBI layer and if GBT forward biased then it becomes temperature dependent. Same results were observed while $TmSiO/TiO_2$ was utilized, but in reverse biased condition. This temperature dependency scaled down with high potential fields, because at high fields FNT dominates.

Till 2013 research for GBT is performed in terms of materials (emitter, EBI, BCI, collector) and their respective properties. Variations in GBT performance

is witnessed with amendments in material selections and respective properties. Very less experiment are performed for GBT performance measurements with respect to analog electronics applications. For analog circuits, it is foremost to have minimum base current leakage. Venica *et al.*²³ has studied base current leakage due to backscattering events in BCI in common base configuration. Rise in backscattering shoots-up base current (I_B) consequently drop in current gain (α_F) is analysed. High V_{BE} makes charge carriers tunnelled (FNT) through EBI (SiO_2 -5 nm) normal to graphene²³. Monte-Carlo transport model is developed for simulating GBT by selecting average velocity ($v(x)$) of charge carriers along the direction of motion. Charge carrier concentration ($n(x)$) in EBI is dependent on $v(x)$.

$$n(x) = J_c / q \cdot v(x) \quad \dots (4)$$

As V_{BE} is varied from 4.4 V to 6 V, $n(x)$ is reduced due to large bending in the conduction band of EBI. This bending moved the injection point towards emitter as shown in Fig. 5. Also during GBT simulation using Monte-Carlo tool, injection point in EBI shifted more nearer to emitter for higher values of V_{BE} . When electrons leave EBI interface and enter into BCI interface travelling normal to graphene base, average kinetic energy is very high because of high value of V_{BE} . Increased value of average kinetic energy enhanced rate of backscattering that ultimately contributes in large base current (I_B) and α_F also. Cardinal reason for backscattering behaviour is discontinuity in conduction band of EBI and BCI. Variation in insulator's width on both sides of graphene base and dielectric constant, both also force backscattering nature. If different materials are used for EBI and BCI then difference in electron affinity also degrades α_F . As electrons enters in BCI region

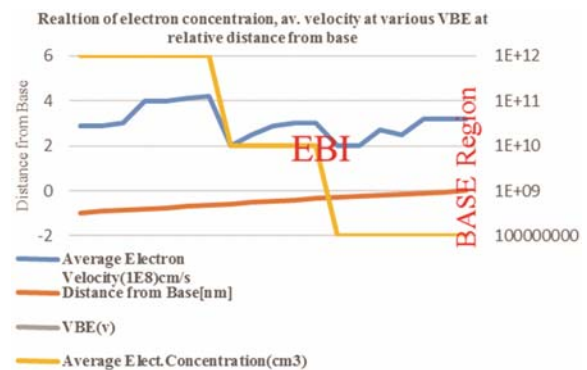


Fig. 5 — Injection point movement with respect to V_{BE} ²³.

with higher electron affinity (χ) (crossing EBI through quantum tunnelling), it becomes tough for electrons to come out of this region. Higher the χ_{BCI} more the energy required to pull put electrons from the surface. For investigating materials variation impact on backscattering and α_F , Venica *et. al.*²³ simulates GBT with SiO₂ as both EBI (1.5 nm-3 nm) and BCI layer (10 nm-20 nm), followed by SiO₂ (5 nm), Al₂O₃ (25 nm) (High-*K* dielectric) as BCI and compared with Driussi *et. al.*²¹. A simulation result for these dimensions divulges that augmentation in V_{BE} in steps of 0.5 V from 4 V to 6.5 V, upsurge in V_{CB} becomes necessity to compensate the drop in α_F .

4 Review of Small Signal Models of GBT and Compact Modelling

Designing of new transistors and the optimization with the intention of developing advanced digital and analog integrated circuit applications, require study of transistor in all regions of operations. To study transistor response for small signal with varying frequencies as inputs, an equivalent representation of transistor is needed. In small signal (SS) equivalent models all parasitic elements are essential, depending on the frequency of operation. GBT’s first SS model for common emitter configuration was developed by Mehr *et.al.*¹³ for power amplifiers. Mehar had proposed two models for low and high frequency of operation. Low frequency SS model is very generic similar to BJT as shown in Fig. 6.

Here in this model ‘E’ represents common emitter terminal with ‘B’ as base input and ‘C’ as collector output. V_1 is the potential drop across output terminal, g_m is trans-conductance, r_π shows dynamic small resistance.

In high frequency (HF) model all parasitic are considered. This HF SS model of GBT is different from BJT HF model. It includes extra parasitic capacitance due to graphene ‘Dirac-point’ energy level as given in Fig. 7. This GBT consists metallic emitter and capacitor. In this model r_π is small dynamic resistance, C_π and C_μ represent parasitic resistances, r_x signifies small base spreading resistance.

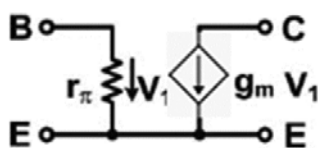


Fig. 6 — SS model of GBT for low frequency¹³.

Lecce *et al.*⁸ has simulated GBT for analog high frequencies signals and proposed a SS model for the same. With the help of this SS model expressions for voltage gain, cut-off frequency and trans-conductance are developed. It is investigated that GBT with voltage gain $A_{vo}= 10$, cannot be scaled below 15-20 nm. Here while simulating GBT as CE amplifier, both voltage gain and cut-off frequency degrades if device total length is scaled below 15 nm. Analyses are performed on undoped silicon for EBI and BCI for t_{BCI} 20 nm and 10 nm with fix t_{EBI} 3 nm. SS model for CE configuration is shown in Fig. 8.

This model is valid only for saturation region. This SS model is developed for higher frequencies as it includes effects of all parasitic that are active at high frequencies. This model is different from the model proposed by Mehr *et al.*¹³, in respect to V_{DE} (graphene Dirac-point energy and emitter Fermi level potential difference). Here author does not work directly with V_{BE} and V_{CE} , rather combination of ‘Dirac-point’ energy with applied base emitter potential (V_{DE}) and base collector potential (V_{DC}) has been used. Because of graphene ‘Dirac-point’ potential (graphene Dirac potential) parasitic capacitances that exist in CE-BJT (Fig. 9) are modified in case of CE-GBT. C_{DE} -parasitic capacitance due to potential difference between base (graphene) of Fermi level and ‘Dirac-point’) similar to C_π . C_μ is modified as C_{DC} potential difference between ‘Dirac-point’ to collector Fermi-level. A new parasitic, as high frequency component due to ‘Dirac-point’ energy, is shown between V_{BE} and V_{DE} , i.e., C_Q .

In Fig. 9, ‘D’ represents ‘Dirac-point’ potential, $g_{BEV_{DE}}$, $j\omega C_n$, $j\omega C_\mu$ and $g_m V_{DE}$ are the voltage

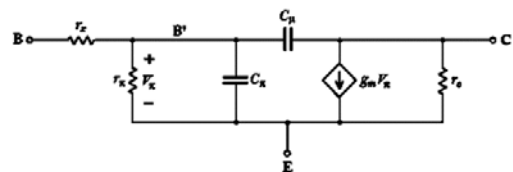


Fig. 7 — HF SS-model for GBT¹³.

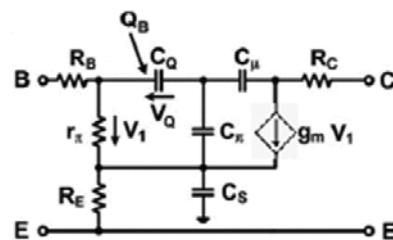


Fig. 8 — Small signal equivalent circuit⁸.

controlled current sources, C_Q , and C_{DC} are the parasitic capacitances. Actually this model is developed using E .

Based on these concepts dependence of I_C on V_{DE} not V_{BE} :

$$I_C = I_C(V_{DE}) \quad \dots (5)$$

By applying Kirchoff's current law at node D in Fig. 5 gives v_{DE} :

$$v_{DE} = \frac{v_{BE}C_Q + v_{CE}(C_{DC} - C_n)}{C_Q + C_{DE} + C_{DC} - C_m - C_n} \quad \dots (6)$$

For this CE- configuration voltage gain that comes out is given by Eq. (7):

$$A_{v_o} = \frac{c_Q}{c_{DC} - c_n} \quad \dots (7)$$

This gain is function of output conductance which is dependent of BCI thickness (t_{BCI}). If t_{BCI} is reduced that means transient time τ_{CB} less, that results in higher I_C for lower V_{CE} ¹⁷. Ultimately reduction in BCI width shots I_C to larger value at cost of drop in voltage gain. It is observed that as GBT scaled role of additive capacitance (C_n , C_m and C_{DC}) becomes prerequisite to incorporate for precise calculation of gain and cut-off frequency. For circuit level evaluation of GBT, model given in Fig. 6 is modified to have large signal model with the help of Ebberts Moll model by Frégonèse *et al.*¹⁷. For circuit level implementation and performance estimation this model is implemented in Verilog-A.

5 Conclusions

Modulations in GBT performance for variation in various materials and related parameters are analysed. All available simulated results of various authors have taken into account for the examination of interdependence of heterogeneous material properties. Insulator's width, relative permittivity, electron affinity, material work function for emitter, collector, insulators and applied potential are performance controlling aspects. No fix criteria are discovered for selection of these parameters. A value of these parameters for best performance in terahertz region varies depending upon material for emitter, collector and insulators. It is concluded that high 'K' provides better collector current density, but applied base emitter potential has to vary accordingly. Simultaneously, effects of cold electrons have to be nullifying through step tunnelling technique. Larger insulator thickness allows choosing lower value of 'K' for same performance. Other than 'K', doping

concentration of emitter will dominate if it is semiconductor material instead of pure metal. To avoid backscattering V_{BE} is not allowed to be much larger. In addition to physical and physics specifications, review of small signal model for CE and CB configuration will guide researchers to model GBT for improved current gain α_F , trans-conductance, and higher operating frequency. This relative study will convey researcher to choose finest device structure with optimized performance.

References

- 1 Colwell R, *IEEE Hot Chips*, 25th Symposium, (2013) 1.
- 2 Roy K, Mukhopadhyay S & Mahmoodi-Meimand H, *IEEE*, 91 (2003) 305.
- 3 Chan C Y, *IEEE VLSI Technol*, (2011) 1.
- 4 <http://wccftech.com/intel-abandoning-silicon-7nm/>
- 5 Wu H, Conrad, Wei Luo & Ye P D, *IEEE Int Electron Devices Meeting, San Francisco, CA*, 9.3.1-9.3.4, (2014).
- 6 Paussa A, Geromel M, Palestri P, Bresciani M, Esseni D & Selmi L, *IEDM Technical Digest*, 11.7.1-11.7.4, (2011).
- 7 Koswatta S O, Valdes-Garcia V, Steiner M B, Lin Y M & Avouris P, *IEEE Trans Microwave Theory Techn*, 59 (2011) 2739.
- 8 Lecce V D, Grassi R, Gnudi A, Gnani E & Baccarani, *IEEE Trans Electron Dev*, (2013) 3493.
- 9 Vaziri S, Belete M, Smith A D, Dentoni L E, Lupina G, Lemme M & Östling, *Nanoscale*, 7 (2015) 13096.
- 10 Cheng R, Bai J, Liao L, Zhou H, Chen Y, Liu L, Lina Y C, Jiang S, Huang Y & Duan X, *Proceedings of the National Academy of Sciences of the United States of America*, 109.29 (2012) 11588.
- 11 Tan M L & Lentaris G, *Nanoscale Res Lett*, 7 (2012) 1.
- 12 Johari Z, Hamid F K, Tan M L, Ahmadi M T, Harun F K & Ismail R, *J Comput Theor Nanosci*, 10 (2013) 1164.
- 13 Mehr W, Dabrowski J, Scheytt C, Xie Y H, Lemme M C, Ostling & Lupina G, *IEEE Electron Dev Lett*, (2012) 33.
- 14 Venica S, Driussi F, Palestri P & Selmi L, *Information and communication technology, electronics and microelectronics*, 37th International Convention, (2014) 33.
- 15 Mead C A, *Proc IRE*, 48 (1960) 359.
- 16 Mead C A, *J Appl Phys*, 32 (1961) 646.
- 17 Frégonèse S, Venica S, Driussi F & Zimmer T, *Electronics*, 4 (2015) 969.
- 18 Vaziri S, Lupina G, Henkel C, Smith A D, Östling M, Dabrowski J, Lippert G, Mehr W & Lemme M C, *Nano Lett*, 13 (2013) 1435.
- 19 Li X, Cai W, An J, Kim S, Nah J, Yang D, Piner R, Velamakanni A, Jung I, Tutuc E, Banerjee S K, Colombo L & Ruoff R S, *Science*, 324 (2009) 1312.
- 20 Lin Y C, Jin C, Lee J C, Jen S F, Suenaga K & Chiu P W, *ACS Nano*, 5 (2011) 2362.
- 21 Driussi F, Palestri P & Selmi L, *Microelectron Eng*, 109 (2013) 338.
- 22 Vaziri S, Belete M, Smith A D, Litta E D, Lupina G, Lemme M C & Östling M, *IEEE 45th European solid state device research conference*, (2015) 198.
- 23 Venica S, Driussi F, Palestri P & Selmi L, *Microelectron Eng*, 168 (2015) 192.