Indian Journal of Pure & Applied Physics
Vol. 57, January 2019, pp. 52-62

High input impedance *trans*-admittance mode biquad universal filter employing DVCCTAs and grounded passive elements

Chandra Shankar[a]* & Sajai Vir Singh[b]

[a]Department of Electronics Engineering, J S S Academy of Technical Education, Noida 201 301, India
[b]Department of Electronics and Communications, Jaypee Institute of Information Technology, Noida 201 304, India

Received 13 October 2017; accepted 11 July 2018

In this paper a new high input impedance *trans*-admittance-mode biquad filter has been proposed and investigated which has been designed using two differential voltage current conveyor *trans*-conductance amplifiers (DVCCTAs) and all grounded passive elements in the form of two capacitors and three resistors only. The proposed TAM filter has the ability to realize all five standard filtering functions, simultaneously. Apart from these characteristics, the proposed filter also enjoys the desirable features such as low active and passive sensitivities, low power consumption, high impedance for both input voltage and output current signal and orthogonal electronic tunability of pole frequency and quality factor. The overall performance of the presented filter has been investigated using mathematical analysis, pre-layout and post-layout simulation results obtained by PSPICE in 0.18 μm CMOS process technology.

Keywords: DVCCTA, TAM, Electronic tunability, Biquad, Filter, SIMO

1 Introduction

Over the past few decades, the current-mode approach of signal processing in the design of analogue filters has received ever increasing popularity and remarkable attention over voltage-mode approach[1]. Therefore, each day more and more current-mode (CM) active blocks and their applications in filter design have been proposed and examined by the number of researchers. Current conveyors and their different modified variants such as CCI, CCII, DDCCII, DVCCII, FTFN, CDBA etc., were initially proposed and studied in the literature[1-12]. However, the circuits based on these active elements cannot offer the electronic adjustment properties which may require in number of adjustable applications such as music synthesis, automatic control and speech synthesis to compensate for deviation due to process tolerance, parasitic, temperature, aging, etc[12]. So later on, few more active building blocks having the attractive feature of the electronic adjustment properties such as OTA, CCCII, CFTA, CCTA, CDTA, VDTA, CCCCTA, DDCCTA and DVCCTA etc. were further proposed in the literature[13-40]. Besides it, as applications, numerous biquad filters operated in different modes also exist in the literature[3-11,13-30,32,33,38-41]. Among them the filter operated with voltage input and current output signal called as *trans*-admittance-mode (TAM) filter is worthy of research and special interest as they can be used as an interface circuit connecting voltage mode circuit to current mode circuit whose applications are found in many electronic circuits such as receiver base band block of modern radio system, D/A converter and optical receiver[8]. The TAM filters reported in past have been further classified as single input multi output (called SIMO) and multi input single output (called MISO) on the basis of whether they are using single input signal or multiple copies of input. The detail comparative discussions[8-10,14-27] of both categories of TAM type have been summarized in Table 1. The MISO TAM filters can't realize multi-filtering functions, simultaneously and requires multiple copies of the input signals and hence, require additional buffers (hardware) to obtain the multiple copies of the input signals. Although, they can generally provide all five filtering functions but only one at a time by appropriate selection of the input signal(s)[15-17,19,27]. Apart from this, they usually requires more than one matching condition(s)[15-17,27], and injection of input signal from one terminal of passive element which results in using floating passive elements [15-17,19,27]. On the other hand, the

*Corresponding author (E-mail: porwalchandra@gmail.com)

Table1 — Comparison of different available TAM filter topologies with proposed TAM filter circuit.

References Features	[8]	[9]	[10]	[14]	[15]	[16]	[17]	[18]	[19]	[20]	[21]	[22]	[23]	[24]	[25]	[26]	[27]		Proposed
Configuration Type	SIMO	SIMO	SIMO	SIMO	MISO	MISO	MISO	SIMO	MISO	SIMO	SIMO	SIMO	SIMO	SIMO	SIMO	SIMO	SIMO	MISO	SIMO
No. & type of active element	3 CCII	5 DCC-DVCC	3 FTFN	3 CCCII	2 CDTA	3 CCTA	2 VDTA	2 VDTA	1 DVCC TA	4 OTA	4 OTA	1 VDTA	2 VDTA	1 VDTA	2 CCCC TA	2 CCCC TA	2 VDTA	2 VDTA	2 DVCCTA
No. & types of passive element	3R, 2C	1R , 2C	3R, 2C	2C	2R, 2C	2C	2R, 2C	2C	2R, 2C	2C	2C	1R, 2C	2C	1R, 2C	3C	2C	2C	2C	2C,3R
No. of Floating passive element	4 (2R +2C)	3(2R +1C)	4 (2R +2C)	NIL	3(2R, 1C)	2C	1C	NIL	2(1R, 1C)	NIL	NIL	1C	NIL	1 R	NIL	1 C	NIL	1 C	NIL
Voltage at high impedance	NO	YES	NO	YES	NO	NO	NO	YES	NO	YES	YES	NO	YES	NO	NO	YES	YES	Not all	YES
Realization type	LP, BP, HP	LP, BP, HP	LP, BP,HP	ALL FIVE	ALL FIVE	ALL FIVE	ALL FIVE	LP, BP, HP	ALL FIVE	LP, BP, HP	LP, BP, HP	LP, BP, HP, BR	LP,BP, HP	BP, HP	ALL FIVE	LP, BP, HP	ALL FIVE	ALL FIVE	ALL FIVE
Explicit output	YES	YES	YES	YES	YES	YES	YES	NO	YES	YES	YES	NO	NO	NO	YES	NO	YES	YES	YES
Orthogonal electronic tunability of ω_0 and Q_0	NO	NO	NO	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES
Matching Condition(s) Required	NO	NO	NO	NO	BR, AP	BR, AP	BR, AP	No	AP	NO	NO	NO	NO	NO	BR, AP	NO	BR, AP	BR, AP	AP
Operating Frequency	22.5 KHz	--	15.9 KHz	--	159 KHz	6.28 MHz	2.51 MHz	7.7 MHz	1.09 MHz	0.844 MHz	3 MHz	3.94 MHz	--	2.51 MHz	27.7 KHz	1.63 MHz	1 MHz	1 MHz	13 MHz
Layout Design and Area Calculation	NO	NO	NO	NO	NO	NO	NO	NO	NO	NO	NO	NO	NO	NO	NO	NO	NO	NO	YES 42.2 nm^2
High Q_0 value through electronic means	NO	NO	NO	NO	NO	NO	NO	YES	YES	YES	NO	YES	YES	NO	NO	NO	YES	YES	YES

SIMO type TAM filter with using of single input only, can realize multiple filtering functions simultaneously which increases their adaptability in the wide variety of practical applications[8-10,14,18,20-27]. A number of SIMO types TAM filters based on different active elements such as CCII[8], DVCC[9], FTFN[10], CCCII[14], OTAs[20,21], VDTA[18,22-24,27], CCCCTA[25,26] can be noticed in Table 1. However, these circuits still suffer one or more following drawbacks:

(i) Consisting of more number of active and /or passive elements[8-10,14, 20-21].

(ii) Employing floating passive components[8-10,22,24] and hence, not suitable for fabrication point of view[41].

(iii) Unavailability of voltage input signal at high input impedance terminal[8,10,22,24-25].

(iv) Incompetent of realizing all five standard filtering functions[8-10,18,20-24,26].

(v) Suffering from lack of electronic tunability of filter parameters[8-10].

(vi) Consisting of more than minimum number of capacitors (two) required for realizing various filtering functions[25].

(vii) Not providing explicitly current outputs at high impedance output terminals[18,22-24,26].

(viii) Requiring matching conditions to realize at least two filtering functions, generally, BR and AP responses[25,27].

(ix) None of the circuit has provided chip layout and chip area[8-10,14,18,20-27].

(x) Incompatible of obtaining high quality factor (Q_0) value through electronic means[8-10,14,21,24-26].

In this paper, a new TAM filter circuit based on DVCCTA is proposed which is competent of simultaneously realizing all five filtering functions and does not require any scaled/inversion voltage input for realizing the filtering functions. In addition, the proposed filter employs five grounded passive elements in the form of two capacitors and three resistors which is easier to fabricate in fully integrated circuits. Besides, the proposed circuit also offers few more advantages features such as; low active and passive sensitivities, low power consumption, orthogonal electronic tunability of pole frequency and quality factor and high impedance for the input voltage signal. The validity of proposed filter is also verified by simulating it through PSPICE.

2 DVCCTA Description

The DVCCTA, a recently introduced CM active element, contains well known active element DVCC at input stage followed by OTA at output stage[31]. After its inception, the element has been used in designing of various analog signal processing blocks such as biquad filters[32,33], oscillators[34,35], floating inductors[36], versatile modulator[37], etc. The symbolic diagram of DVCCTA is shown in Fig. 1 which has two high input impedance ports Y_1, Y_2 and one low input impedance port X. Beside it, Z is auxiliary output port whose voltage is transferred to current at

trans-conductance type high impedance output ports (O-). The voltage and current relationship between various ports of DVCCTA can be characterized by following matrix equation:

$$\begin{bmatrix} I_{Y1} \\ I_{Y2} \\ V_X \\ I_Z \\ I_{O-} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 1 & -1 & 0 \\ 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & -g_m \end{bmatrix} \begin{bmatrix} I_X \\ V_{Y1} \\ V_{Y2} \\ V_Z \end{bmatrix} \quad \ldots (1)$$

Where, g_m is the *trans*-conductance parameter of DVCCTA. A CMOS model of DVCCTA consisting of only twenty four transistors is also shown in Fig. 2. For the CMOS circuit of DVCCTA of Fig. 2, the dependency of g_m on biasing current of DVCCTA (I_B) can be expressed as[31]:

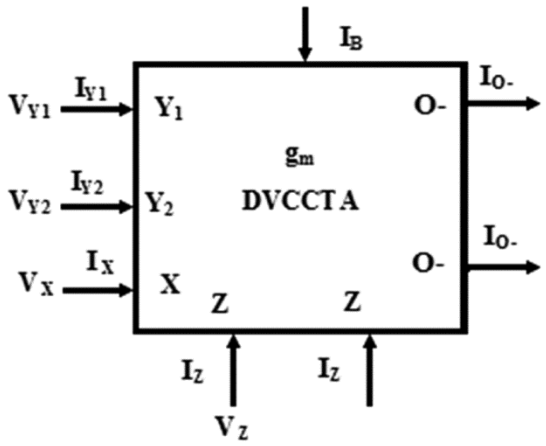


Fig. 1 – Symbolic diagram of DVCCTA.

$$g_m = \sqrt{\mu C_{ox} \left(\frac{W}{L}\right)_{M14,M15} I_B} \quad \ldots (2)$$

Here μ is the effective carrier mobility, C_{ox} is the gate oxide capacitance per unit area, and W and L are the effective channel width and length of the M_{14} and M_{15} MOS transistor.

3 Proposed TAM Filter and Analysis

The proposed TAM filter topology is shown in Fig. 3 which employs two DVCCTAs, three grounded resistors (R_1, R_2, and R_3) which may be realized by using two NMOS transistors[17], and two grounded capacitors (C_1 and C_2). Routine analysis of the circuit in Fig. 3 yields three transfer functions of LP, BP and BR in *trans*-admittance mode across explicitly available current outputs I_{LP}, I_{BP}, and I_{BR}, respectively which can be expressed mathematically as:

$$TAM_{LP}(s) = \frac{I_{LP}}{V_{in}} = \frac{\left(\frac{g_{m2}}{C_1 C_2 R_2 R_3}\right)}{D(s)} \quad \ldots (3)$$

$$TAM_{BP}(s) = \frac{I_{BP}}{V_{in}} = \frac{s\left(\frac{g_{m1}}{C_1 R_2}\right)}{D(s)} \quad \ldots (4)$$

$$TAM_{BR}(s) = \frac{I_{BR}}{V_{in}} = -\frac{\frac{1}{R_2}\left(s^2 + \frac{g_{m2}}{C_1 C_2 R_3}\right)}{D(s)} \quad \ldots (5)$$

In addition of LP, BP and BR, the HP response can also be obtained by adding currents I_{LP} and I_{BR}, together. So the *trans*-admittance mode HP response can be expressed as:

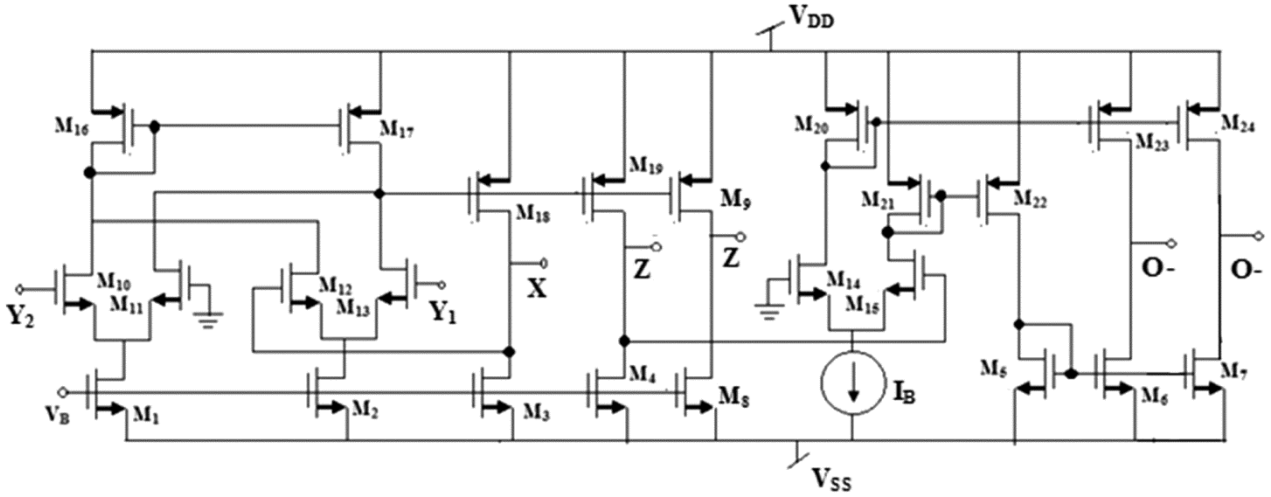


Fig. 2 – CMOS implementation of DVCCTA.

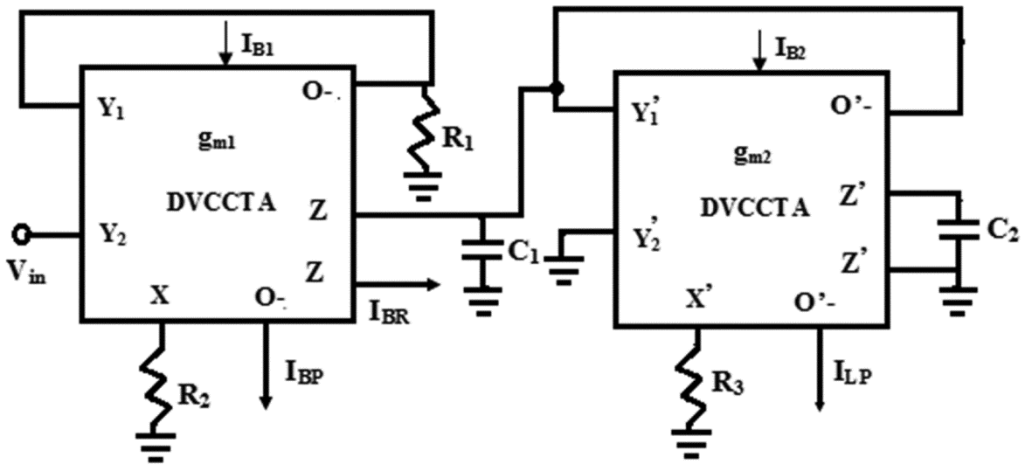


Fig. 3 – Block diagram of proposed TAM biquad filter.

$$TAM_{HP}(s)=\frac{I_{HP}}{V_{in}}=\frac{I_{LP}+I_{BR}}{V_{in}}=-\frac{s^2\left(\frac{1}{R_2}\right)}{D(s)} \quad \ldots (6)$$

Similarly, AP response can also be realized simply by adding currents I_{BP} and I_{BR}. So *trans*-admittance mode AP response can be expressed as:

$$TAM_{AP}(s)=\frac{I_{AP}}{V_{in}}=\frac{I_{BP}+I_{BR}}{V_{in}}=-\frac{\frac{1}{R_2}\left(s^2-s\frac{g_{m1}}{C_1}+\frac{g_{m2}}{C_1C_2R_3}\right)}{D(s)} \quad \ldots (7)$$

$$\text{where, } D(s)=\left[s^2+s\frac{g_{m1}R_1}{C_1R_2}+\frac{g_{m2}}{C_1C_2R_3}\right] \quad \ldots (8)$$

It can be noted that from Eqs (3)-(7) that the proposed topology is capable of realizing *trans*-admittance-mode LP, BP, HP, BR and AP filtering responses. However, AP filtering response requires a matching condition $R_1 = R_2$ which can be easily satisfied. Further, the characteristic parameters of proposed filter like pole frequency (ω_0), quality factor (Q_0), and bandwidth (BW) can be derived as:

$$\omega_0=\sqrt{\frac{g_{m2}}{C_1C_2R_3}} \quad \ldots (9)$$

$$Q_0=\frac{R_2}{g_{m1}R_1}\sqrt{\frac{g_{m2}C_1}{C_2R_3}} \quad \ldots (10)$$

$$BW=\frac{g_{m1}R_1}{C_1R_2} \quad \ldots (11)$$

It can be concluded from Eqs (9)–(10) that the Q_0 can be varied electronically and independent of ω_0 by varying g_{m1} (I_{B1}) only. Similarly, the ω_0 can also be varied electronically without affecting Q_0 by varying g_{m2} and also by maintaining the condition as $g_{m1}= g_{m2} = 1/R_3$. As the grounded resistor(s) can be realized through two NMOS transistors so R_3 can be further tuned through electronic means[17].

4 Non Ideal Effects and Sensitivities Analysis

After considering the effects of non-ideal characteristics of the DVCCTA[31], the current and voltage relationship between various ports of DVCCTA can be rewritten as:

$$\begin{bmatrix} I_{Y1} \\ I_{Y2} \\ V_X \\ I_Z \\ I_{O-} \end{bmatrix}=\begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & \gamma & -\gamma & 0 \\ \alpha & 0 & 0 & 0 \\ 0 & 0 & 0 & -\beta g_m \end{bmatrix}\begin{bmatrix} I_X \\ V_{Y1} \\ V_{Y2} \\ V_Z \end{bmatrix} \quad \ldots (12)$$

where α, β, and γ are the tracking errors and their values are nearly equal to one. Considering the above non ideal errors discussed in Eq. (12), we have further reanalyzed the proposed circuit of Fig. 3. On analyzing, the non-ideal filter transfer functions and its filter parameters can be derived as follow:

$$TAM_{LP}(s)=\frac{I_{LP}}{V_{in}}=\frac{\left(\frac{\alpha_1\alpha_2\gamma_1\gamma_2\beta_2 g_{m2}}{C_1C_2R_2R_3}\right)}{D'(s)} \quad \ldots (13)$$

$$TAM_{BP}(s)=\frac{I_{BP}}{V_{in}}=\frac{\left(\frac{s\alpha_1\beta_1\gamma_1 g_{m1}}{C_1R_2}\right)}{D^{'}(s)} \quad \ldots (14)$$

$$TAM_{BR}(s)=\frac{I_{BR}}{V_{in}}=-\frac{\frac{\alpha_1\gamma_1}{R_2}\left(s^2+\frac{\alpha_2\beta_2\gamma_2 g_{m2}}{C_1C_2R_3}\right)}{D^{'}(s)} \quad \ldots (15)$$

$$TAM_{HP}(s)=\frac{I_{HP}}{V_{in}}=-\frac{s^2\left(\frac{\alpha_1\gamma_1}{R_2}\right)}{D^{'}(s)} \quad \ldots (16)$$

where,

$$D^{'}(s)=\left[s^2+s\frac{\alpha_1\beta_1\gamma_1 g_{m1}R_1}{C_1R_2}+\frac{\alpha_2\beta_2\gamma_2 g_{m2}}{C_1C_2R_3}\right] \quad \ldots (17)$$

$$\omega_0^{'}=\sqrt{\frac{\alpha_2\beta_2\gamma_2 g_{m2}}{C_1C_2R_3}} \quad \ldots (18)$$

$$TAM_{AP}(s)=\frac{I_{AP}}{V_{in}}=-\frac{\frac{\alpha_1\gamma_1}{R_2}\left(s^2-s\frac{\alpha_2\beta_2\gamma_2 g_{m1}}{C_1}+\frac{\beta_1 g_{m2}}{C_1C_2R_3}\right)}{D^{'}(s)} \quad \ldots (19)$$

$$Q_0^{'}=\frac{R_2}{\alpha_1\beta_1\gamma_1 g_{m1}R_1}\sqrt{\frac{\alpha_2\beta_2\gamma_2 g_{m2}C_1}{C_2R_3}} \quad \ldots (20)$$

$$BW^{'}=\frac{\alpha_1\beta_1\gamma_1 g_{m1}R_1}{C_1R_2} \quad \ldots (21)$$

It is evident from Eqs (13) - (21) that the filter parameters such as pass band gain of various filtering responses, ω_0, Q_0, and BW of the proposed TAM filter may be slightly changed due to effect of tracking errors of DVCCTA but these deviation can be minimized by adjusting the electronic controllable *trans*-conductance parameters.

The active and passive sensitivities of ω_0 and Q_0 for the proposed filter in Fig. 3 can also be derived as follow:

$$S^{\omega_0^{'}}_{\alpha_2,\beta_2,\gamma_2,g_{m2}}=\frac{1}{2}, S^{\omega_0^{'}}_{C_1,C_2,R_3}=-\frac{1}{2} \quad \ldots (22)$$

$$S^{Q_0}_{g_{m2},C_1,\alpha_2,\beta_2,\gamma_2}=\frac{1}{2}, S^{Q_0}_{C_2,R_2}=-\frac{1}{2}, S^{Q_0}_{g_{m1},R_1,\alpha_1,\beta_1,\gamma_1}=-1, S^{Q_0}_{R_2}=1 \quad \ldots (23)$$

From above Eqs (22) and (23), it can be noted that all the active and passive sensitivities of ω_0 and Q_0 are low and equal or less than 'unity' in magnitude.

5 Non Ideal Parasitic Analysis

In this section, the effect of DVCCTA parasitics on the performance of presented TAM filter is considered. In the presence of various ports parasitic in the form of parasitic capacitors and resistors, the circuit of Fig. 3 has been changed to Fig. 4. In Fig. 4 the external resistances R_1, R_2, R_3 and parasitic resistances R_{Pi} (i= 1, 2, 3, 4, 5) are represented in terms of admittances as G_1, G_2, G_3 and G_{Pi} (i = 1, 2, 3, 4, 5), respectively, (where $G_i = 1/R_i$, $G_{Pi} = 1/R_{Pi}$). In Fig. 4, the parasitics can be seen as a parallel combination of resistors and capacitors at combined ports (Z_1, Y_1', O_1-') as $C_{P1}||G_{P1}$, at port Z' as $C_{P2}||G_{P2}$, at combined ports (Y_1, O_1-) as $C_{P3}||G_{P3}$, and as a series parasitic impedenace at port X as G_{P4}, at port X' as G_{P5}. The Practical value of parasitic capacitances (C_{Pi}) are found in the range of fraction of picofarads and parasitic admittances are in the range of tens of micromho. Therefore, min (C_1, C_2)>> (C_{P1}, C_{P2}, C_{P3},) and min (G_1, G_2)>> (G_{P1}, G_{P2}, G_{P3}, G_{P4} , G_{P5}). After reanalysing the circuit of Fig. 4, to see the effects of various parasitic impedances on the performance of

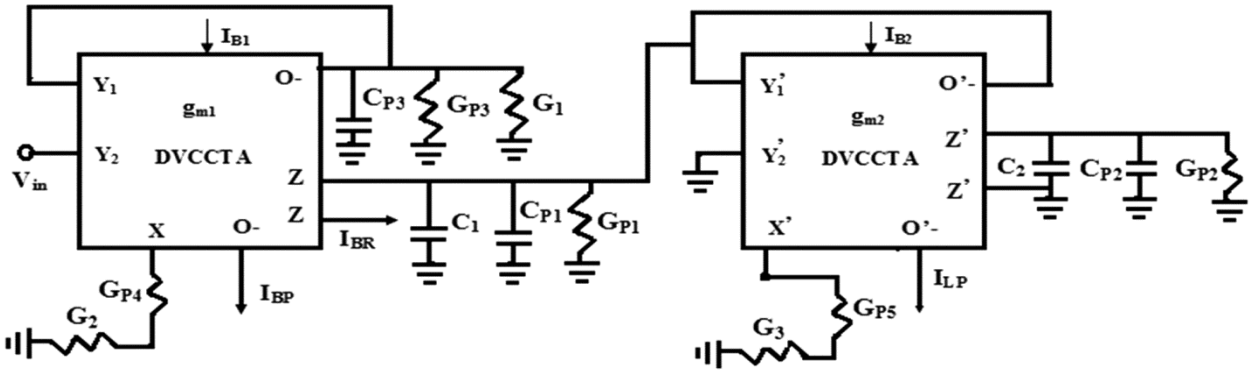


Fig. 4 – Proposed biquad filter in the presence of various ports parasitic.

the proposed TAM filter circuit, the following transfer functions for the TAM filtering functions can be obtained as:

$$TAM_{LP}(s)=\frac{I_{LP}^{"}}{V_{in}}=\frac{\frac{g_{m2}G_2G_3}{C_1C_2}\left(1+\frac{sC_{P3}}{G_3}\right)V_{in}}{\left(1+\frac{G_{P2}}{sC_2}\right)D^{"}(s)} \quad \ldots (24)$$

$$TAM_{BP}(s)=\frac{I_{BP}^{"}}{V_{in}}=\frac{sg_{m1}\frac{G_2}{C_1}\left(1+\frac{sC_{P3}}{G_1}\right)}{D^{"}(s)} \quad \ldots (25)$$

$$TAM_{BR}(s)=\frac{I_{BR}^{"}}{V_{in}}=-\frac{G_2\left(1+\frac{sC_{P3}}{G_1}\right)\left[s^2\left(1+\frac{G_{P2}}{sC_2}\right)\left(1+\frac{G_{P1}}{sC_1}\right)+\frac{g_{m2}G_3}{C_1C_2}\right]}{\left(1+\frac{G_{P2}}{sC_2}\right)D^{*}(s)}$$

$\ldots$ (26)

$$TAM_{HP}(s)=\frac{I_{HP}^{"}}{V_{in}}=-\frac{\left[s^2G_2\left(1+\frac{sC_{P3}}{G_1}\right)\left(1+\frac{G_{P1}}{sC_1}\right)\right]}{D^{*}(s)} \quad \ldots (27)$$

$$TAM_{AP}(s)=\frac{I_{AP}^{"}}{V_{in}}=$$

$$-\frac{\frac{G_2}{C_1}\left(1+\frac{sC_{P3}}{G_1}\right)\left(s^2C_1\left(1+\frac{G_{P2}}{sC_2}\right)\left(1+\frac{G_{P1}}{sC_1}\right)-sg_{m1}\left(1+\frac{G_{P2}}{sC_2}\right)+\frac{G_3g_{m2}}{C_2}\right)}{\left(1+\frac{G_{P2}}{sC_2}\right)D^{*}(s)}$$

$\ldots$ (28)

where,

$$D^{*}(s)=\left[s^2\left(1+\frac{sC_{P3}}{G_1}\right)+s\frac{g_{m1}G_2}{C_1G_1}+\frac{g_{m2}G_3}{C_1C_2}\right] \quad \ldots (29)$$

As a result, expressions of pole frequency and quality factor have been changed to:

$$\omega_0^{"}=\omega_0\sqrt{\frac{1}{1+s\left(\frac{C_{P3}}{G_1}\right)}} \quad \ldots (30)$$

$$Q_0^{"}=Q_0\sqrt{1+s\left(\frac{C_{P3}}{G_1}\right)} \quad \ldots (31)$$

where ω_0 and Q_0 are the pole frequency and quality factor of the TAM filter in ideal case. It can be clearly seen from Eqs (24) – (31) that additional first order poles and zero are yielded in the expression of transfer functions and filter parameters due to various port parasitic of DVCCTA which may deviate undesirably the pass band gain, pole frequency and quality factor of the proposed filter. However, these undesirable factors can be eliminated or minimized and hence, the proposed filter may approach towards ideal response, if we choose the operating frequency (ω_0) in the design criterion as follows:

Condition

$$\max\left(\frac{G_{P1}}{C_1},\frac{G_{P2}}{C_2}\right)<<\omega<<\min\left(\frac{G_1}{C_{P3}}\right) \quad \ldots (32)$$

6 Effects of Frequency Dependent Parameter (g_m) on Performance of Proposed Filter and Stability Analysis

DVCCTA is a bandwidth limited device due to frequency dependent parameter *trans*-conductance gain (g_m), so the stability of proposed filter may be affected due to the bandwidth limitation of g_m. Suppose g_m depends only on single pole frequency ω_p which can be expressed as:

$$g_m=\frac{g_{mo}}{1+\frac{s}{\omega_p}}=g_{mo}\frac{\omega_p}{s+\omega_p}\cong g_{mo}\left(1-s\tau\right),\omega\tau<<1 \quad \ldots (33)$$

On using Eq. (33) and further re-analysing the proposed filter, the following transfer functions of various TAM responses and their filter parameters can be obtained as:

$$TAM_{LP}(s)=\frac{I_{LP}^{'''}}{V_{in}}=\frac{\left(\frac{g_{m02}(1-s\tau_2)}{C_1C_2R_2R_3}\right)}{D(s)} \quad \ldots (34)$$

$$TAM_{BP}(s)=\frac{I_{BP}^{'''}}{V_{in}}=\frac{s\left(\frac{g_{m01}(1-s\tau_1)}{C_1R_2}\right)}{D(s)} \quad \ldots (35)$$

$$TAM_{BR}(s)=\frac{I_{BR}^{'''}}{V_{in}}=-\frac{\frac{1}{R_2}\left(s^2+\frac{g_{m02}(1-s\tau_2)}{C_1C_2R_3}\right)}{D(s)} \quad \ldots (36)$$

$$TAM_{HP}(s)=\frac{I_{HP}^{'''}}{V_{in}}=-\frac{s^2\left(\frac{1}{R_2}\right)}{D(s)} \quad \ldots (37)$$

$$TAM_{AP}(s)=\frac{I_{AP}^{'''}}{V_{in}}=$$

$$-\frac{\frac{1}{R_2}\left(s^2\left(1+\frac{g_{m01}\tau_1}{C_1}\right)-s\left(\frac{g_{m01}}{C_1}+\frac{g_{m02}\tau_2}{C_1C_2R_3}\right)+\frac{g_{m02}}{C_1C_2R_3}\right)}{D(s)}$$

$\cdots$ (38)

where

$$D'''(s)=\left[s^2\left(1-\frac{g_{m01}\tau_1 R_1}{C_1R_2}\right)+s\left(\frac{g_{m01}R_1}{C_1R_2}-\frac{g_{m02}\tau_2}{C_1C_2R_3}\right)+\frac{g_{m02}}{C_1C_2R_3}\right] \quad \ldots (39)$$

$$\omega_0'''=\sqrt{\frac{\frac{g_{m02}}{C_1C_2R_3}}{\left(1-\frac{g_{m01}\tau_1R_1}{C_1R_2}\right)}} \quad \ldots (40)$$

$$Q'''_0=\frac{\sqrt{\frac{g_{m02}}{C_1C_2R_3}\left(1-\frac{g_{m01}\tau_1R_1}{C_1R_2}\right)}}{\left(\frac{g_{m01}R_1}{C_1R_2}-\frac{g_{m02}\tau_2}{C_1C_2R_3}\right)} \quad \ldots (41)$$

where g_{m01} and g_{m02} are the *trans*-conductance parameter of DVCCTA1 and DVCCTA2, respectively, at zero frequency. From Eq. (39), it can be observed that stability problem of proposed filter is found due to bandwidth limitation of g_m of DVCCTA as pole(s) of the characteristic Eq. (39) may lie on right hand side of *s*-plane. However, the proposed filter can be made stable by satisfying the following conditions which can be achieved easily as:

$$\tau_1 << \frac{C_1R_2}{g_{m01}R_1} \text{ and } \tau_2 << \frac{g_{m01}C_2R_1R_3}{g_{m02}R_2} \quad \ldots (42)$$

7 Simulation Results

7.1 Pre-layout simulation

In order to check the performance, the presented filter was designed using CMOS implementation of DVCCTA with calculated aspect ratio of transistor as described in Table 2 and pre-layout simulation simulations were carried out using PSPICE in ORCAD 16.5 with model of 0.18 µm CMOS process parameters. The proposed circuit was biased with power supply voltages of V_{DD} = -V_{SS} = 1.4 V, V_B = -0.5 V and designed to obtain the pole frequency of 13.0 MHz. For this designing, the active and passive components values were determined as I_B = 137 µA ($g_m \approx$ 1205 µA/V), R_1 = R_2= 1.5 kΩ, R_3 = 0.8 kΩ, C_1= C_2 = 15 pF. The corresponding simulated as well as ideal gain responses of LP, BP, BR, and HP *trans*-admittance are shown in Fig. 5. It is clear from Fig. 5 that simulated results are in good agreements with the ideal results. Moreover, the simulated pole frequency was obtained 12.70 MHz which is closed to the theoretical value of 13.0 MHz. Figure 6 shows the gain and phase response of AP for the proposed TAM filter. The total power consumption of the filter was obtained as 9.21 mW.

Table 2 — Transistors aspect ratios

Transistor	*W*/*L*	Transistor type
M1-M8	4.32/0.36	NMOS
M10-M13	1.44/0.36	NMOS
M14-M15	21.6/0.36	NMOS
M16-M19,M9	21.6/0.36	PMOS
M20-M24	7.2/0.36	PMOS

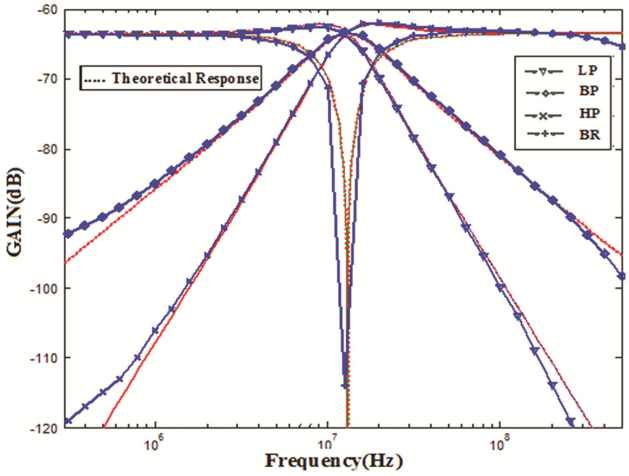


Fig. 5 – Ideal and PSPICE simulated response of LP, HP, BP, and BR TAM filter.

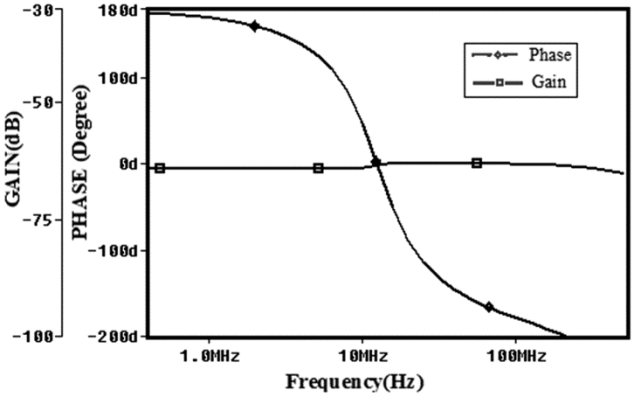


Fig. 6 – Gain and phase response of AP filter.

To show the electronic tuning feature of the proposed filter, the circuit is further simulated to obtain various BP responses at different sets of I_{B1}= I_{B2} (g_{m1} = g_{m2}) as I_{B1} = I_{B2} = 25 µA, 50 µA,100 µA, and 200 µA in such a way so that g_{m1} = g_{m2} = 1/R_3 which result in the pole frequency variation of 3.16 MHz, 5.9 MHz, 10.0 MHz, and 16.2 MHz, respectively, at constant Q_0 = 1. The corresponding simulated result shows the pole frequency tuning feature independent of Q_0 as shown in Fig. 7.

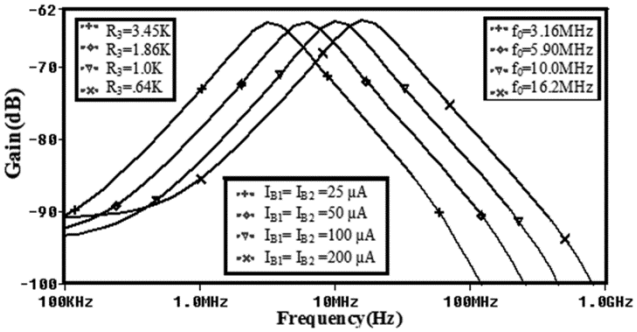


Fig. 7 – Electronic tunability of ω_0 independent Q_0 for TAM BP filter.

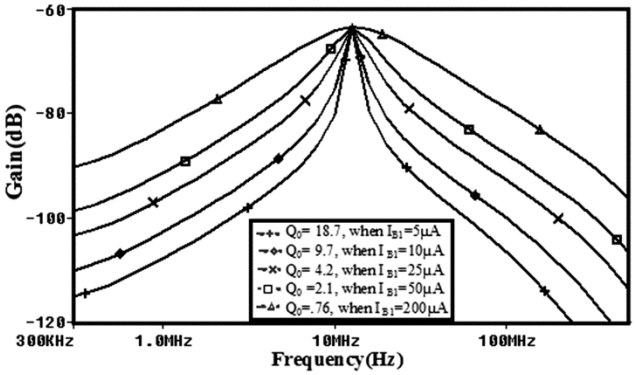


Fig. 8 – Electronic tunability Q_0 independent of ω_0 for TAM BP filter.

Besides it, Fig. 8 also shows the tuning of Q_0 independent of ω_0 by varying g_{m1}, for example; g_{m1} = 64.0 µA/V (I_{B1} = 5 µA), g_{m1} = 124 µA/V (I_{B1} = 10 µA), g_{m1} = 290 µA/V (I_{B1} = 25 µA), g_{m1} = 538 µA/V (I_{B1} = 50 µA), and g_{m1} = 1575 µA/V (I_{B1} = 200 µA) which obtained Q_0 = 18.8, 9.7, 4.2, 2.1, and 0.76, respectively. The simulated values were found nearly same as calculated values such as 19.2, 9.9, 4.23, 2.3, and 0.78, respectively.

Further, the transient behavior of the proposed circuit by applying the sinusoidal input of 5 MHz frequency was also investigated and corresponding simulated output results of LP filter are shown in Fig. 9, which shows the LP output in TAM with respect to applied sinusoidal input voltage signal having peak to peak amplitude of 100 mV. Next, the total harmonic distortions (THDs) of the LP response of the proposed circuit was also measured by applying a sinusoidal current input signal of varying frequency in the range of 500 kHz to 14 MHz at constant peak to peak amplitude of 100 mA. The THDs result is shown in Fig. 10 which shows that the % THD figures are adequate and not more than moderate and acceptable range[37] of 2.8% and causes the LP TAM output not

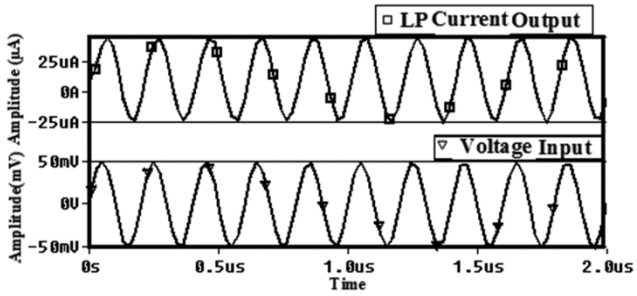


Fig. 9 – Transient response of TAM LP filter.

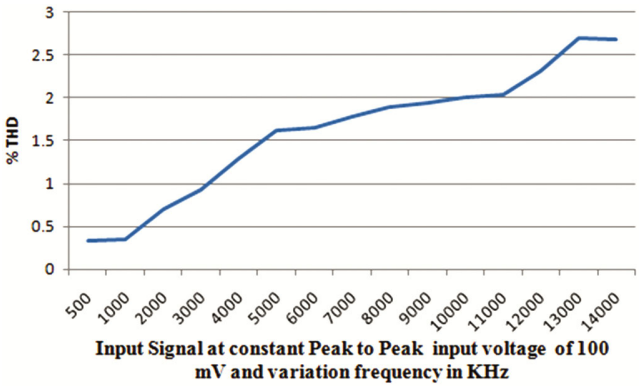


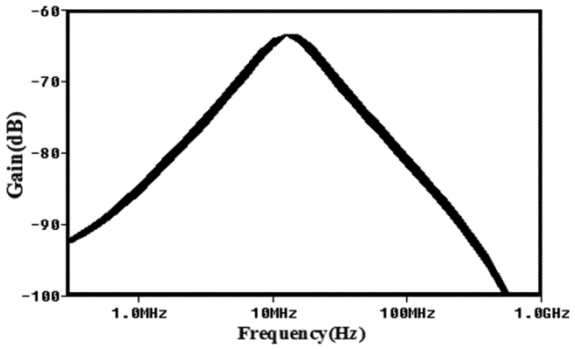
Fig. 10 – % THDs of LP filter at fixed peak to peak input voltage signal of 100 mV.

distorted significantly for an applied sinusoidal voltage input of variable frequency and constant amplitude.

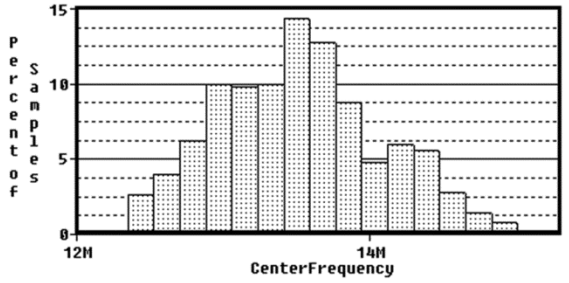
To observe the effect of component mismatching on filter's performance, Monte-Carlo analysis was performed. To measure the impact, the TAM BP output was simulated with 10% Gaussian deviation in C_1 = C_2 = 15 pF for 500 concurrently runs. Corresponding simulated results of BP response are shown in Fig. 11(a) and 11(b). Figure 11(a) shows the magnitude response whereas Fig. 11(b) shows the statistical results in the form of histogram where the simulated mean, median and standard deviation were obtained as 13.52 MHz, 13.50 MHz and 557.76 kHz, respectively, which conclude that with respect to the simulated pole frequency of 12.70 MHz, the proposed filter is less sensitive to the change in capacitive value and thus offers good passive sensitivity.

7.2 Layout designs and post-layout simulation results

In the previous section, all the simulation results were pre-layout simulation results. Now, in this section, post-layout simulations of proposed TAM biquad filter are also carried out using cadence's virtuoso tool to see the parasitic effect which includes all the parasitic capacitances and resistor in the layout.



(a)



n samples	= 500	10th %ile	= 1.28101e+007
n divisions	= 15	median	= 1.35011e+007
mean	= 1.35215e+007	90th %ile	= 1.43234e+007
sigma	= 557760	maximum	= 1.5015e+007
minimum	= 1.23506e+007	3*sigma	= 1.67328e+006

(b)

Fig. 11 – Monte Carlo analysis of TAM biquad filter.

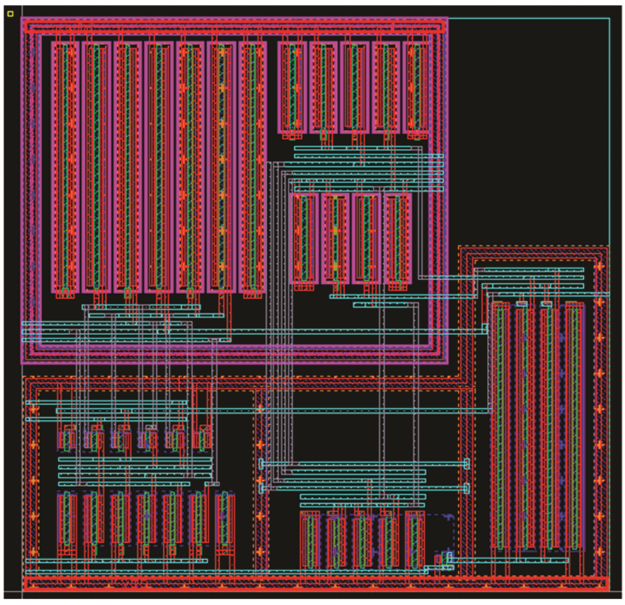


Fig. 12 – Layout of DVCCTA as shown in Fig. 2.

For this purpose, first we have designed the layout of DVCCTA which is shown in Fig. 12. Afterward, the layout of proposed TAM filter with same active and passive components value is designed and shown in Fig. 13. The layout has been verified by using design rule checks (DRC) and layout verses schematic (LVS)

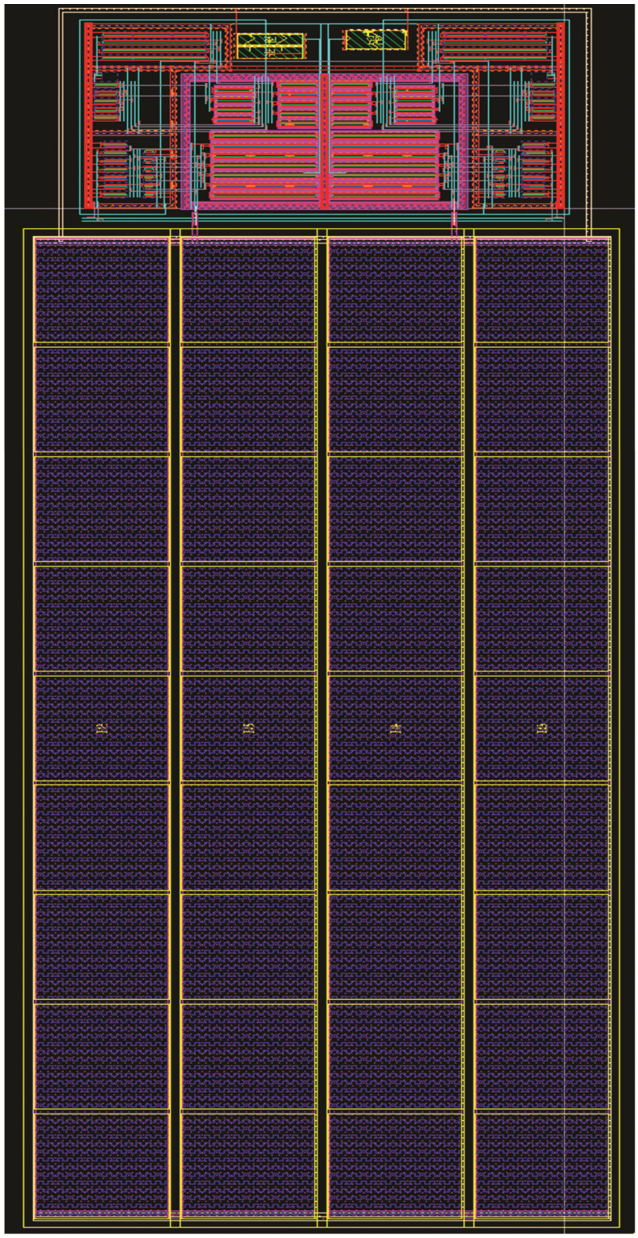


Fig. 13 – Layout design of proposed biquad filter of Fig. 3.

processes which verify the potential errors and nets mismatching between schematic and layout respectively[30]. After these processes parasitic extraction was performed which extract the total parasitic in the design. The parasitic values as described in section 5 as C_{P1}, C_{P2}, and C_{P3} were also calculated 0.057 pF, 0.0225 pF and 0.033pF, respectively. Since parasitic capacitors C_{P1} and C_{P2} are parallel to large value capacitors C_1 and C_2, so these capacitors can be neglected which was also explained theoretically in section 5. The area of CMOS implemented DVCCTA layout and chip area of

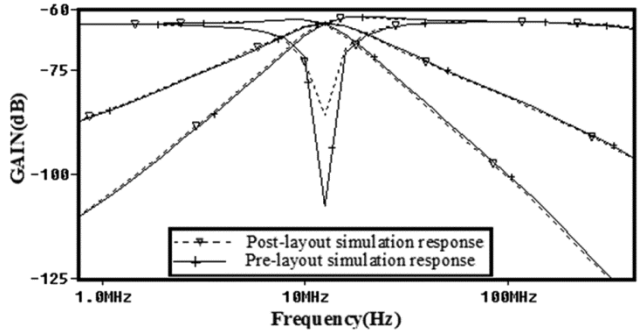


Fig. 14 – Pre-layout and post layout simulation response of LP, HP, BP, and BR TAM filter.

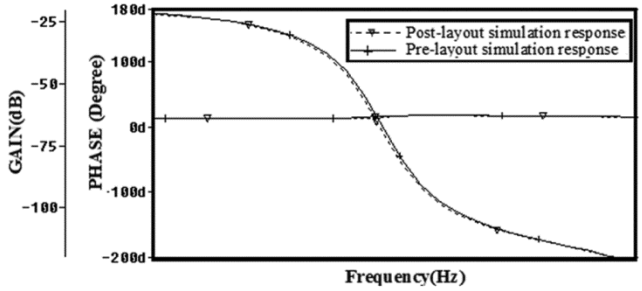


Fig. 15 – Pre-layout and post layout simulation of gain and phase response of AP filter.

biquad filter without pads are found to be 2.62 nm^2 and 42.20 nm^2, respectively. The total power consumption is calculated to be 9.21 mW. Figure 14 and Fig. 15 show the post layout simulation results of the filter in term of frequency responses of LP, BP, BR, HP, and AP responses. The post layout simulation results are almost same with pre-layout simulation results and obtained pole frequency is 12.57 MHz which is nearly same as 12.7 MHz, obtained in pre-layout simulation results.

8 Conclusions

In this paper a new DVCCTA based *trans*-admittance mode biquad filter topology is presented which has the ability of realising all five filtering functions such as the LP, BP, HP, and BR and AP, simultaneously and employs only two DVCCTAs as active element, two grounded capacitors and three grounded resistors for the implementation. Moreover, the presented TAM filter also enjoy with the feature of low active and passive sensitivities, low power consumption, independent electronic tunability of filter parameters, input voltage applied to high input impedance terminal and no requirement of inverting type input signal etc. Beside it, the proposed filter was also analysed to consider the effect of non ideal parameter (α, β, γ), frequency dependent parameter (g_m), stability condition, parasitic resistance and capacitances on the performance of the circuit. Further, both pre-layout and post layout simulation of the proposed circuit has been successively carried out which validate that the presented circuit can be made fully integrable in CMOS technology and ready for chip level fabrication. The chip area of biquad filter without pads is found to be 42.20 nm^2. The above distinguished features and analysis of the circuit make hope that this work will add to the body of knowledge on classical filter design.

References

1 Toumazou C, Lidgey F J & Marks C A, *IEE Proc G - Circuits Dev Syst*, 137 (1990) 116.
2 Smith K C, *Proc IEEE*, 56 (1968) 1368.
3 Soliman A M, *Circuits Syst Signal Process*, 27 (2008) 405.
4 Minai S & Ibrahim M A, *Int J Circuits Theory Appl*, 37 (2003) 793.
5 ChiuW Y & Horng J W, C*ircuits Syst Signal Process*, 31 (2012) 19.
6 EI-Adaway A A, Soliman A M & Elwan H O, *Analog Digital Signal Process*, 47 (2000) 306.
7 Sagbal M & Köksal M A, *New multi-mode multifunction filter using CDBA*, Circuit Theory and Design, Proceedings of the European Conference 2, 2005.
8 Toker A, Çicekoglu O, Özcan S & Kuntman H, *Int J Electron*, 88 (2001) 1085.
9 Beg P, Maheshwari S & Siddiqi M, *IET Circuits Dev Syst*, 7 (2013) 193.
10 Pandey N & Paul S K, *J Circuits Syst*, 1 (2010) 54.
11 Shah N A, Iqbal S Z & Parveen B, *Analog Integr Circuits Signal Process*, 40 (2004) 87.
12 Papazoglou C & Karybakas C, *IEE Proc Circuits Dev Syst*, 144 (1997) 178.
13 Biolek D, Senani R, Biolkova V & Kolka Z, *Radioeng J*, 17 (2008) 15.
14 Tangsriart W & Surakampontorm W, *Circuits Syst Signal Process*, 25 (2006) 701.
15 Shah N A, Quadri M & Iqbal S Z, *Analog Integr Circuits Signal Process*, 52 (2007) 65.
16 Singh S V, Tomar R S & Chauhan D S, *IJE Trans C: Aspects*, 28 (2015) 1738.
17 Shankar C & Singh S V, *WSEAS Trans Circuits Syst*. 14 (2015) 8.
18 Gupta G, Singh S V & Bhooshan S V, *Circuits Syst*, 6 (2015) 93.
19 Singh S V & Shankar C, *Int J Eng Technol*, 8 (2016) 1671.
20 Bhaskar D R, Singh A K, Sharma A K & Senani R, *IEICE Electron Exp*, 2 (2005) 8.
21 Ibrahim M A & Kuntman H, *A novel trans-admittance-type biquad employing DO-OTA with only two grounded capacitor,* Proceeding of 13th IEEE International Conference Signal Processing and Communications Applications, 2005.
22 Shankar C & Singh S V, *Int J Eng Technol*, 7 (2016) 2180.
23 Prasad D, Srivastava M & Bhaskar D R, *Int Scholar Res Notice*, 2014 (2014) 1.
24 Shankar C & Singh S V, *A low voltage operable VDTA based biquad filter realizing band pass and high pass*

filtering functions in trans-admittance-mode, Proceeding of IEEE conference on Computing, Communication & Automation (ICCCA), 2015.
25 Singh S V, Maheshwari S, Mohan J & Chauhan D S, *An electronically tunable SIMO biquad filter using CCCCTA,* Proceeding of IEEE conference on Communications in Computer and Information Science (CCIS), 2009.
26 Singh S V, Maheshwari S & Chauhan D S, *Int J Recent Trends Eng Technol*, 3 (2010).
27 Yeşil A & Kaçar F, *Radioengineering*, 22 (2013) 1016.
28 Singh S V, Tomar R S & Chauhan D S, *J Eng Sci Technol*, 12 (2017) 2268.
29 Satansup J, Pukkalanun T & Tangsrirat W, *Circuits, Systems Signal Process*, 32 (2012) 945.
30 Chen H P & Yang W S, *Appl Sci*, 7 (2017) 244.
31 Jantakun A, Pisutthipong N & Siripruchyanun M, *A synthesis of temperature insensitive/electronically controllable floating simulators based on DV-CCTAs,* In Proceedings of the 6th International Conference on Electrical Engineering/ Electronics, Computer, Telecommunications and Information Technology, 2009.
32 Pandey N & Paul S K, *Act Pass Electron Comp*, 2011 (2011).
33 Verma K & Gautam S, *Int J Sci Res Eng Technol*, 2 (2013) 93.
34 Tuntrakool S & Jaikla W, *Single DVCCTA based voltage mode quadrature sinusoidal oscillator with electronic controllability,* UKSim-AMSS 8th European Modelling Symposium, 2014.
35 Lahiri A & Jaikala W, *Analog Integr Circuits Signal Process*, 65 (2010) 321.
36 Tangsrirat W, *Indian J Eng Mater Sci*, 20 (2013) 79.
37 Pandey N, Pandey R, Sayal A & Tripathi M, *Act Pass Electron Comp*, 2014 (2014).
38 Chen H P & Wang S F, *Int J Electron Commun*, 70 (2016) 491.
39 Prasad D, Bhaskar D R & Srivastava M, *Indian J Pure Appl Phys*, 51 (2013) 864.
40 Singh S V & Shankar C, *J Eng Sci Technol*, 13(1) (2018) 280.
41 Tuntrakool S, Kumngern M, Sotner R, Herencsar N, Suwanjan P & Jaikla W, *Indian J Pure Appl Phys*, 55 (2017) 324.