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# Novel methods to reduce leakage current in Si PIN photodiodes designed and fabricated with different dielectrics

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The silicon PIN photodiodes were designed and fabricated in the conventional bipolar planar technology by using novel methods to reduce the leakage current. The new process steps like gettering, oxide stacking fault removing, ion implantation with suitable masking and improving shallow junction technology were implemented to fabricate PIN photodiodes of different active area such as 1 mm × 1 mm, 2 mm × 2 mm and 10 mm × 10 mm. The performance of PIN photodiodes has been studied by measuring dark current, *C-V* characteristics and spectral response. The two different dielectrics such as silicon dioxide ($SiO_2$) and silicon nitride ($Si_3N_4$) with different thickness were used as anti-reflective coating (ARC). The electrical characteristics and spectral measurements exhibit that the photodiodes are highly sensitive with low leakage current.

**Keywords:** Si PIN photodiode, Silicon dioxide, Silicon nitride, *I-V*, *C-V* characteristics, Spectral response

## 1 Introduction

Silicon PIN diode and PIN photodiodes are used to detect different ionizing radiations like X-rays, γ-rays, electrons and heavy ions[1]. The Si PIN photodiode performance is comparable with that of other detectors such as scintillation detectors, gas filled detectors, ionization chambers and thermo-luminescent detectors. The Si PIN photodiodes are less expensive and exhibit better quality when compared to the conventional detectors. The advantages of Si PIN photodiodes are small in size, fast response, better energy resolution and can operate at room temperature. The technique involved in the fabrication of Si PIN photodiodes is the conventional silicon fabrication process[2,3]. These standard semiconductor processes can be used in the fabrication of Si based PIN type radiation detectors. The radiation detectors can be fabricated in different structures such as circles, strips, micro strips and double-sided strip detectors. The PIN photodiodes are used to measure the position of the incident radiation and the pixel PIN photodiodes are used as radiation image sensors. Therefore, the Si PIN photodiodes of different active area and shapes are used in pre-shower detector of compact muon solenoid (CMS) in large hadron collider (LHC) at CERN, Geneva, Switzerland[4-6].

The capability of Si PIN photodiodes to detect X-rays makes them a competent contender to use in X-ray scanners in security systems. The Si PIN photodiodes are also used in short distance communication and optical storage systems which require fast and sensitive photo detectors with low dark current[7-9]. The performance of a PIN photodiode is essentially enhanced by reducing the surface reflectance[10] of the ARC. The use of optimum ARC on the surface of the photodiode can increase the quantum efficiency as high as 80% at the peak wavelength of response region[11]. A single layer ARC is the most efficient system since it allows reduction in reflectance only in a narrow wavelength domain of the solar spectrum[12,13]. Therefore, it is essential to develop Si PIN photodiodes with low dark current with maximum quantum efficiency for different applications. An ARC thickness plays an important role in reducing the dark current and to increase the quantum efficiency. Therefore, the effect of ARC thickness on different electrical characteristics and spectral response of different active area Si PIN photodiodes have been investigated in the present paper. The $SiO_2$ and $Si_3N_4$ are used separately as anti-reflective coatings and the thickness of ARC is varied from 50 to 250 nm. The comparison of *I-V*, *C-V* and spectral response results are presented and discussed in this paper.

### 1.1 Design and Simulation

The PIN photodiodes with different active area of 1 $mm^2$, 4 $mm^2$ and 100 $mm^2$ were designed using Cadence design tool. The schematic diagrams (top view) of the different active area PIN photodiodes are shown in Fig. 1. The red coloured dots as seen in the Figure 1(C) for 100 $mm^2$ device indicate the top aluminium contact and the similar contacts are also present in other area devices. The active area of the photodiode is coated with 50, 100, 150 and 250 nm thickness of silicon dioxide ($SiO_2$) as anti-reflective coating (ARC). The active area of photodiode is also coated with 50 and 250 nm thickness of $Si_3N_4$ as ARC. The photodiodes without ARC coating were also fabricated to study the spectral response of pristine PIN photodiode.

Silvaco process simulation tools were used to design the process parameters such as surface concentration, junction depth and doping profile. The several thermal cycles were chosen and the suitable thermal cycle was selected based on 1-D simulation studies. The process parameters were optimized to achieve the required electrical parameters like low leakage current, higher breakdown voltage and the better spectral response. The representative doping profile of Si PIN photodiode with $SiO_2$ is shown in Fig. 2 and the similar doping profile was observed for $Si_3N_4$ ARC devices.

### 1.2 Device technology and fabrication process

The photodiodes were fabricated at IC fabrication facility having class 1000/100 environment available at Bharat Electronics Limited (BEL), Bangalore. The diffusion process, ion implantation process and over all process integration were tuned to optimize the photodiode performance.

### 1.3 Substrate

The *n*-type phosphorus doped 4 inch (100 mm) silicon wafers with <111> orientation were considered for the fabrication of Si PIN photodiodes. These are float zone (FZ) type high purity silicon wafers having carrier life time greater than 1 ms. The wafer thickness was 450 µm after double side polish and the resistivity is 5-8 kΩ-cm. The face of the wafer on which the photodiode is fabricated is conventionally considered as 'top' and the other face as 'bottom.'

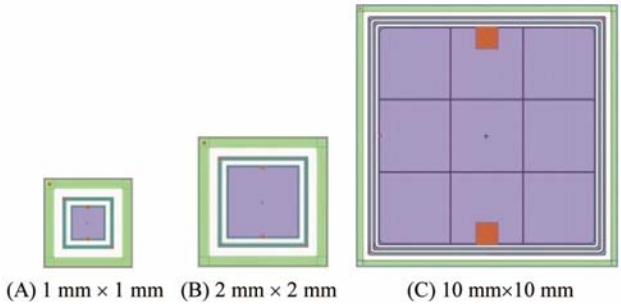


Fig. 1 — Schematic diagram of the different active area PIN photodiode designed using cadence design tools

### 1.4 Initial preparation of wafer

The sacrificial oxide thickness of 0.4 µm ($T_{OX}$) was grown on the top of silicon wafer. The sacrificial oxide removes the surface defects on the silicon wafer and this process ensures a defect free surface for further fabrication processes. The gettering process was performed at the bottom of the silicon wafer to reduce the bulk defects and the top side sacrificial oxide layer was completely etched at room temperature using buffer oxide etchant solution ($HF:NH_4F$).

### 1.5 Bottom $N^+$ process

A 0.4 µm thick initial oxide layer was grown on the top side of the silicon wafer in the furnace. At the bottom side of the wafer, phosphorous (P) ions were implanted and annealed at 1100°C to have bottom $N^+$ contact. The sheet resistance after $N^+$ process was found to be 8-10 Ω/ϒ. The P ion implantation and annealing would provide good ohmic contact at the bottom of the silicon wafer.

### 1.6 Patterning before $P^+$ layer

The top $P^+$ pattern was created using photo-lithography. The steps involved in the photo-

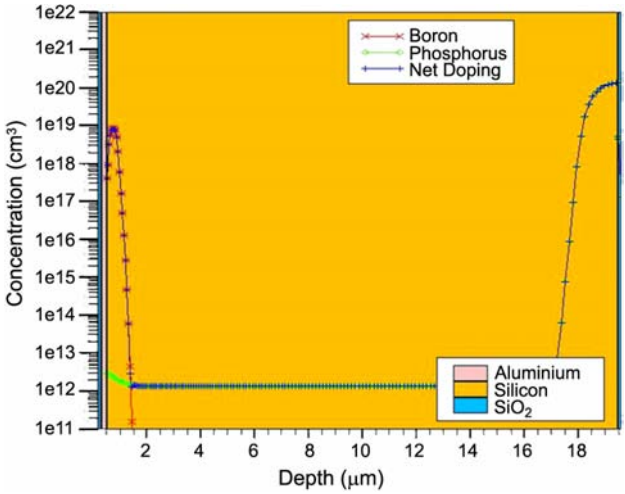


Fig. 2 — Simulated doping profile of Si PIN photodiode

lithography are describes as follows: first the negative photo resist HNR 120 was coated on the wafers and were exposed to UV light in Contact/proximity Mask Aligner (CA 600) using a $P^+$ pattern mask and further developing was done using Waycoat Negative Developer. After rinsing and drying, the wafers were inspected for proper alignment and proper developing of the patterns.

The inspected wafers were baked at 150°C in $N_2$ ambient to remove solution and to make the hard photo-resist. The oxide etching was performed to get the required patterns in the silicon wafers. The post etching inspection was carried out to ensure the complete etching and the photo-resist was removed using $H_2SO_4$ and $H_2O_2$ solutions (Caros acid). The rinsing and drying of the wafers were done using deionised water to remove the acid content. Again, the wafer inspection was done to ensure the designed patterns before the next processing steps.

#### 1.7 Screen oxidation

A thin layer of $SiO_2$ of thickness 50 nm was thermally grown as masking/screen oxide for implantation. The thermally grown oxide (TGO) reduces the channelling effect during implantation and also reduces the surface damage. The thin $SiO_2$ layer assists the further deposition of $SiO_2$ and $Si_3N_4$ as anti-reflective coating.

#### 1.8 $P^+$ doping by implantation

The boron ions were implanted using a high current implanter to form *p*-type layer on *n*-type substrate. The $P^+$ implantation was done at room temperature in high vacuum with implantation energy of 80 keV with beam current of few μA. The *p*-type dopants are annealed in the temperature range 900°-1000°C to reactivate the dopant ions and restore the crystal lattice. During the annealing process, the junction depth of 1-2 μm of $P^+$ layer concentration is achieved. The junction depth was confirmed by measurements using CSM Calotest industrial instrument. The sheet resistance of $P^+$ layer was measured by four point probe method (model Veeco FPP-100) and it was found to be in the range 240-260 Ω/ϒ.

#### 1.9 Contact photo lithography and aluminium deposition

The contacts were opened in the $P^+$ areas using photolithography process and contact mask. The native oxide was removed by pre-metal etching and the wafers were subjected to RCA cleaning to remove the organic and inorganic contaminations. The aluminium metal of thickness in the range 0.2-0.3 μm was deposited using Varian sputtering system. After lithography, aluminium metal contacts were provided for $p^+$ and $n^+$ layers as shown in Fig. 3.

#### 1.10 Anti-reflective coating (ARC)

The $SiO_2$ and $Si_3N_4$ are individually deposited as anti-reflective coating on the top side and the ARC of different thickness was deposited on different wafers. The each geometry photodiodes have $SiO_2$ thickness of 50, 100, 150 and 250 nm and $Si_3N_4$ thickness of 50 and 150 nm. The ARC will act as the passivation layer to the chip to protect from moisture and mechanical damages. The schematic cross-section of photodiode after completion of fabrication is shown in Fig. 3.

The initial fabrication process steps were adopted from the conventional bipolar planar process. In addition to this, in order to reduce the leakage current the following innovative concepts were adopted in the fabrication processes.

- The surface defects and contamination on the surface of the wafer were reduced by introducing the sacrificial oxidation process.
- The defects generated during oxidation process will increase the leakage current and reduce the breakdown voltage. In order to reduce the oxide-induced defects, pyrogenic-oxidation is performed using Trans 1-2 dichloro-ethylene (Trans LC) as gettering agent. The Trans LC gives better results when compared to other gettering agents like HCl and TCA.
- The defects in the bulk of silicon were reduced by ion implantation process at the bottom of the wafer. The ion implantation is repeated twice with two

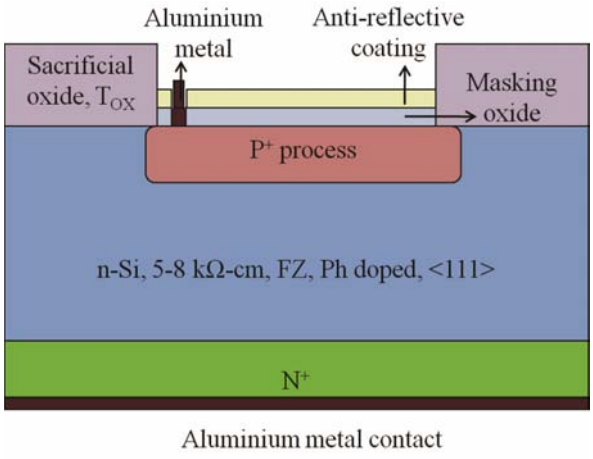


Fig. 3 — Cross-sectional view of Si PIN photodiode

different ion species having different doses and energies. The ion species and ion energies were optimized after repeated trials. The advantage of having $N^+$ ion implantation and gettering process at the bottom of the wafer helps to increase the charge collection efficiency of $N^-$region.

- Ion implantation process introduces channeling effect in the wafer and damages the silicon surface. Several trails were conducted with different oxide thickness and the screen oxide of 50 nm was introduced to avoid channeling effects.
- The leakage paths will be generated in the masking field oxide due to boron ions trapped in the oxide during $P^+$ implantation process. In order to avoid the leakage paths, photo-resist was retained on the masking field oxide. The photo-resist will act as a mask on the field oxide and prevent the boron contamination in the field oxide area during boron ion implantation.
- The process has been optimized to get low leakage current in junction detectors by maintaining low leakage currents and high break-down voltages.

## 2 Results and Discussion

The reverse bias current of Si PIN photodiodes should be low for radiation detection. Therefore, change in the reverse bias current has been studied for monitoring the operating performance of Si PIN photodiode. In an ideal PIN photodiode, the leakage current is the direct evidence of diffusion current but practically, in addition to diffusion current, photodiodes comprises of leakage currents from the impurities, contaminations, process induced defects and interface states at $Si/SiO_2$ interface[14]. The maximum current generated by a pulse of radiation will produce around 1 μA of leakage current in less than pico-seconds. When the Si PIN photodiodes are working in the radiation environment, the leakage current should be minimal in order to detect the incident radiation. Therefore, it is important to design and fabricate a detector with the leakage current less than 1 nA/cm$^2$ at the typical bias voltage of-10 V. When photodiodes are exposed to ionizing radiation, the leakage current increases by several orders of magnitude[15]. Therefore, it is essential to measure the reverse biased leakage current of different active area Si PIN photodiodes deposited with different thickness of ARC. The fabrication processes have been optimised to obtain the minimum leakage current in the order of few nA/cm$^2$. The variations in reverse biased leakage current for photodiodes deposited with different ARC thickness have been studied at wafer level. The reverse biased breakdown voltage of the Si PIN photodiodes was found to be around-250 V. The thermally grown masking/screen oxide (TGO) of 50 nm is not sufficient to prevent the photodiode from mechanical damages and moisture. An optimum ARC thickness should be provided with minimum leakage current and without any compromise in the spectral response.

Figures 4-6 show the comparison of leakage current for $SiO_2$ and $Si_3N_4$ deposited photodiodes with active area 1 mm$^2$, 4 mm$^2$ and 100 mm$^2$, respectively. From Figs 4-6, it is evident that the leakage current is very low for photodiodes with 50 nm TGO when compared to different ARC thickness. However, the leakage current increases with $SiO_2$ and $Si_3N_4$ deposition. The leakage current is more for PIN photodiodes deposited with $SiO_2$ when compared to photodiodes deposited with $Si_3N_4$. In $SiO_2$ deposited photodiodes,

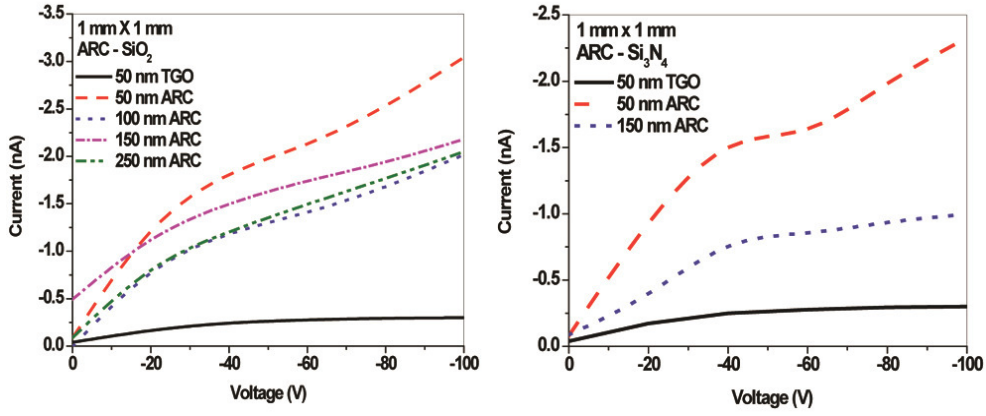


Fig. 4 — Variation in leakage current as a function of ARC thickness in 1 mm$^2$ active area PIN photodiode

the porosity in $SiO_2$ and the interface states at $Si/SiO_2$ interface are the main reasons for the observed high leakage current. In TGO, very few silicon dangling bonds at the $Si/SiO_2$ interface result in small leakage current. But more number of silicon dangling bonds at the TGO-$SiO_2$ or TGO-$Si_3N_4$ interface contribute to the more leakage current when compared to photodiodes deposited without any ARC. The *I-V* characteristics of all the photodiodes deposited with ARC show that the leakage current is in nA range. It can be seen from Figs 4-6 that the leakage current increases with increase in active area of the photodiode. The leakage currents are prominent for higher active area photodiodes which show that the edge generation is more dominant in higher active area photodiodes.

The capacitance of PIN photodiode in reverse bias condition is given by the equation; $C = dQ/dV = \varepsilon A/X$ where the charge $Q = q\ N_{eff}\ AX$, where $A$ is the diode area, $N_{eff}$ is effective dopant concentration and $X$ is the depletion depth. The capacitance decreases proportionally to $1/\sqrt{V}$ until the full depletion is achieved. For applied bias voltages larger than the full depletion voltage, the capacitance remains constant and a plateau region can be observed. The capacitance at full depletion voltage corresponds to the geometrical capacitance of the diode which is considered as a parallel plane plate capacitor[16]. Figures 7-9 show the comparison of capacitance measured for photodiodes with active area of 1 $mm^2$, 4 $mm^2$ and 100 $mm^2$, respectively. The capacitance increases with increase in active area of the photodiode and the capacitance increases up to the geometrical capacitance of the photodiode (Figs 7-9). The capacitance of the photodiode starts saturating at −20 V and the photodiode becomes fully depleted. The capacitance of the PIN photodiodes is well within pF range and the capacitance will be minimum for depletion voltage. The minimum capacitance value corresponds to the bulk capacitance of the PIN

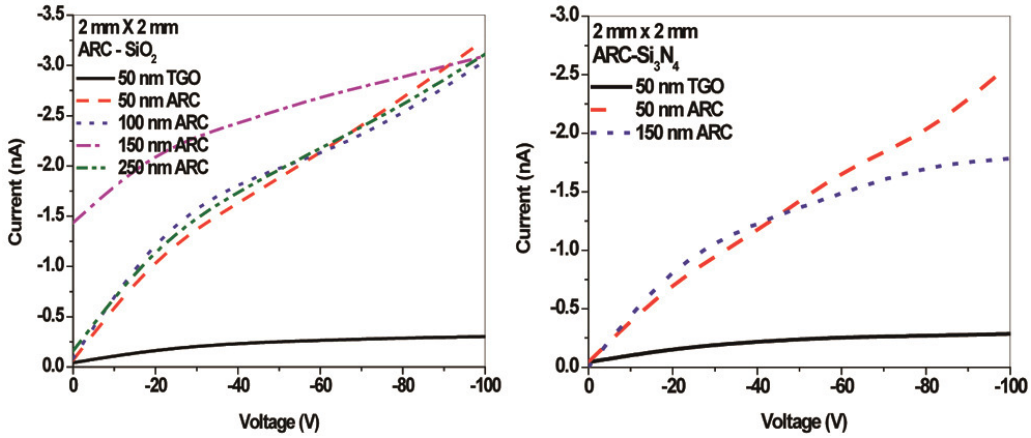


Fig. 5 — Variation in leakage current as a function of ARC thickness in 4 $mm^2$ active area PIN photodiode

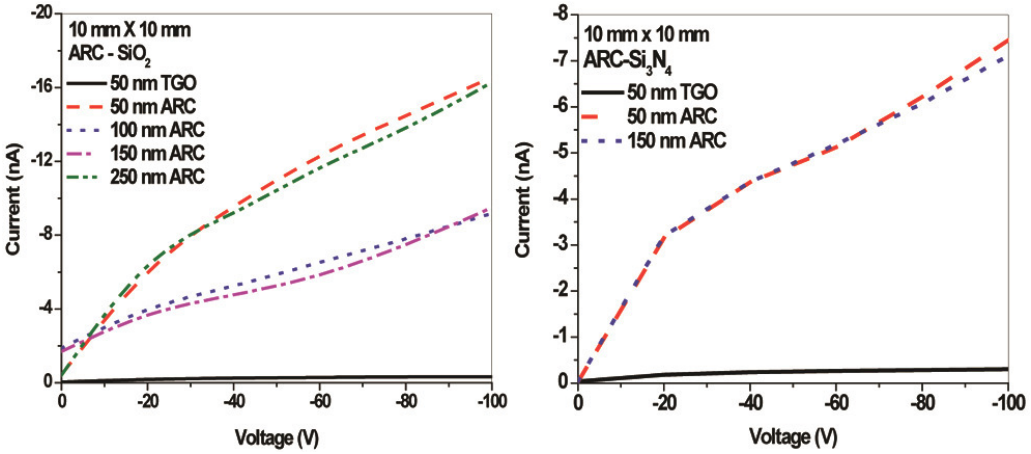


Fig. 6 — Variation in leakage current as a function of ARC thickness in 100 $mm^2$ active area PIN photodiode

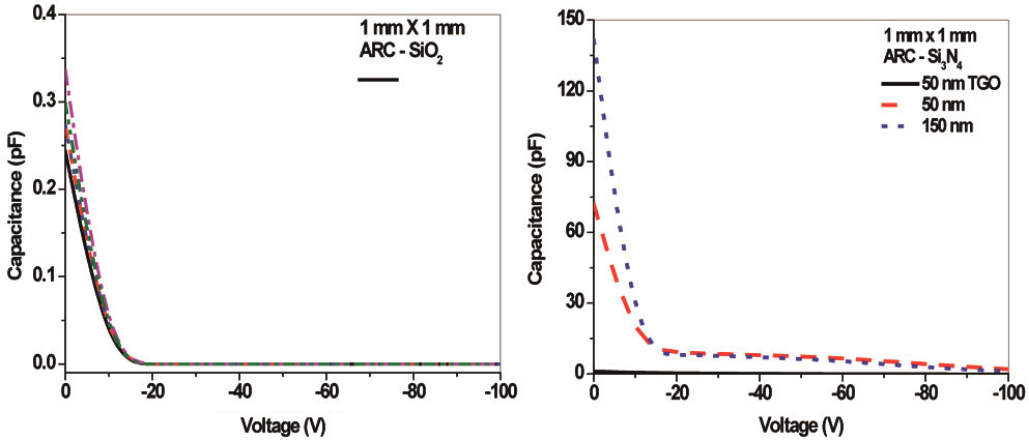


Fig. 7 — Capacitance-voltage characteristics as a function of ARC thickness in 1 $mm^2$ active area PIN photodiode

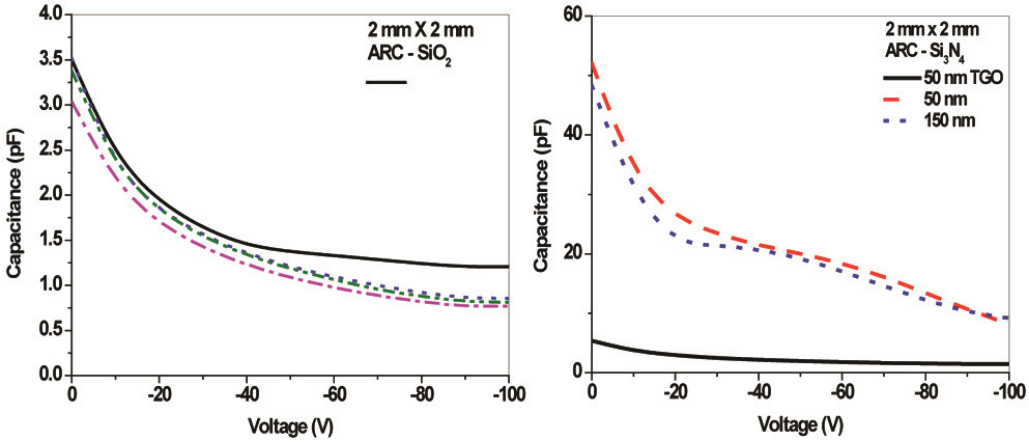


Fig. 8 — Capacitance-voltage characteristics as a function of ARC thickness in 4 $mm^2$ active area PIN photodiode

photodiode. At voltages higher than the depletion voltage, the capacitance corresponds to the dielectrics thickness. The relative permittivity of $Si_3N_4$ is more than the relative permittivity of $SiO_2$ hence, the capacitance of $Si_3N_4$ deposited photodiodes is more when compared to $SiO_2$ deposited photodiodes. However, photodiodes deposited contain $SiO_2$ as TGO before $Si_3N_4$ and therefore, two dielectrics are present as ARC. The difference between the capacitance of two dielectrics is seen as a small hump in the *C-V* curve at about −50 V for photodiodes deposited with $Si_3N_4$.

Figure 10 shows the spectral response for 1 $mm^2$ PIN photodiodes and the similar results were observed for 4 $mm^2$ and 100 $mm^2$ photodiodes. The spectral response of PIN photodiodes has been studied by operating the photodiode in photoconductive mode. The photo response of PIN photodiodes is in the visible and near-infrared region. The peak spectral response is around 950 nm for different active area photodiodes deposited with different ARC thickness and there is no shift in the peak spectral response. The amount of energy lost by the photons is negligible for the $SiO_2$ thickness between 50 nm to 250 nm. Therefore, there is no drastic change in the spectral response for the $SiO_2$ thicknesses between 50 nm to 250 nm. But the spectral response of the $Si_3N_4$ deposited devices decreases with increase in $Si_3N_4$ thickness as seen in Fig. 10. The energy of the incident radiation is lost in the $Si_3N_4$ layer and hence, the spectral response decreases. The increasing thickness in $Si_3N_4$ layer attenuates the incident radiation and therefore, the spectral sensitivity of the photodiode decreases. Therefore, $SiO_2$ acts as better protective layer than $Si_3N_4$ and with increasing $SiO_2$ thickness spectral response remains unchanged.

The study of *I-V*, *C-V* and spectral response characteristics show that the PIN photodiodes operate

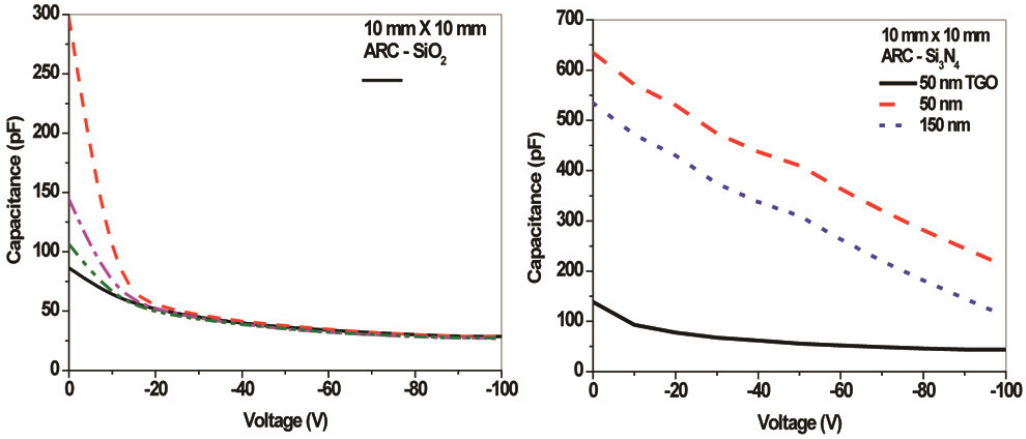


Fig. 9 — Capacitance-voltage characteristics as a function of ARC thickness in 100 mm$^2$ active area PIN photodiode

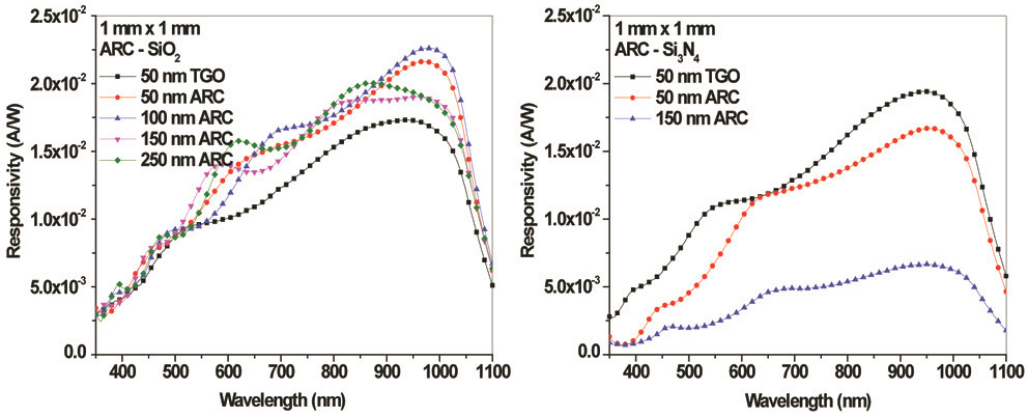


Fig. 10 — Variation in spectral response as a function of ARC thickness in 1 mm$^2$ active area PIN photodiodes

in the expected wavelength region. The present investigation shows that the optimum $SiO_2$ thickness is between 50 and 150 nm and the optimum $Si_3N_4$ thickness is 50 nm. The higher thickness of $SiO_2$ and $Si_3N_4$ will decrease the spectral response of the PIN photodiode.

## 3 Summary

The PIN photodiodes were designed using Cadence design tools. The 1-D process simulations have been studied to optimise the different process parameters and the PIN photodiodes were fabricated using planar process. The silicon PIN photodiodes of different area were deposited with $SiO_2$ and $Si_3N_4$ of different thickness. The methods like gettering, oxide stacking fault removing, ion implantation with suitable masking and improving shallow junction technology were implemented to obtain low leakage current in PIN photodiode. The *I-V*, *C-V* and spectral response characteristics of Si PIN photodiodes have been studied to understand the effects of different ARC thickness on the performance of photodiodes. The very low leakage currents and high breakdown voltage were achieved in these fabricated PIN photodiodes using novel and innovative concepts in the device fabrication.

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