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Three-input-one-output current-mode universal biquadratic filter using one differential difference current conveyor

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A current-mode universal biquadratic filter is presented. The architecture has three input terminals, one output terminal using one differential difference current conveyor (DDCC), two grounded capacitors and two resistors. It can realize all standard second-order filter functions, which are, highpass, bandpass, lowpass, notch and allpass responses without changing the circuit topology. The proposed circuit employs only one DDCC that simplifies the circuit configuration.

Keywords: Current conveyor, Biquadratic filter, Active circuit, Current-mode

1 Introduction

There is a growing interest in designing current-mode current conveyor (CC) based active filters. This is attributed to their high signal bandwidths, greater linearity and larger dynamic range than OPAMP based ones[1]. It is attractive for filters to employ grounded capacitors because of its easier monolithic IC implementation[2,3]. Several current-mode universal biquadratic filters with multi-inputs have been presented[4-11]. Chang and Chen[4] proposed a current-mode universal biquadratic filter with three inputs and single output using five second-generation current conveyors (CCIIs), two grounded capacitors and six grounded resistors[4]. Chang *et al*[5]. proposed the second current-mode universal biquadratic filter with three inputs and single output using four CCs (two first-generation CCs and two second-generation CCs), two grounded capacitors and two grounded resistors[5]. Chang[6] proposed the third current-mode universal biquadratic filter with three inputs and single output using five plus-type CCIIs, two grounded capacitors and four resistors[6]. Chang and Tu[7] proposed the fourth current-mode universal biquadratic filter with three inputs and single output using four multiple output CCIIs, two grounded capacitors and four grounded resistors[7]. Gunes *et al*[8]. proposed a current-mode universal biquadratic filter with four inputs and single output using three multiple output CCIIs, two grounded capacitors and two grounded resistors[8]. Wang and Lee[9] proposed a current-mode universal biquadratic filter with three inputs and three outputs using two multiple output CCIIs, one multiple output third-generation CC (CCIII), two grounded capacitors and two grounded resistors[9]. Horng[10] proposed a current-mode universal biquadratic filter with five inputs and single output using three CCIIs, two grounded capacitors and three resistors. Horng *et al*[11]. proposed a current-mode universal biquadratic filter with three inputs and single output using one CCII, one multiple output CCIII, two grounded capacitors and two grounded resistors.

Several current-mode universal biquadratic filters with five input terminals have been presented[12-14]. However, the active or passive components used in the design of these multi-inputs current-mode universal filters[4-14] were not minimum.

Kacar *et al*[15]. proposed a current-mode universal biquadratic filter with three inputs and single output using one fully differential current conveyor (FDCCII), two grounded capacitors and two grounded resistors[15]. However, the FDCCII is a very complicated device. On each FDCCII, there are almost twice as many MOSs as one differential difference current conveyor (DDCC) needs. Moreover, the port relations of a FDCCII are equivalent to the port relations of two DDCCs arithmetically.

A new current-mode universal biquadratic filter with three inputs and single output using only one DDCC, two grounded capacitors and two resistors is

presented. The new current-mode circuit can realize all standard filter types. With respect to the multi-inputs current-mode biquads[4-14], the proposed circuit uses less active elements. With respect to the three inputs and single output current-mode biquad[15], the proposed circuit uses simpler active device. A summary of these reported multi-inputs current-mode biquads[4-15] and the proposed filter are given in Table 1.

2 Circuit Description

Using standard notation, the port relations of a DDCC can be described by the following matrix equation[16]:

$$\begin{bmatrix} i_{y1} \\ i_{y2} \\ i_{y3} \\ v_x \\ i_{zk} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 1 & -1 & 1 & 0 & 0 \\ 0 & 0 & 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} v_{y1} \\ v_{y2} \\ v_{y3} \\ i_x \\ v_{zk} \end{bmatrix} \quad \ldots(1)$$

where the plus and minus signs indicate whether the DDCC is configured as a non-inverting or inverting circuit, termed DDCC+ or DDCC-.

The proposed current-mode universal biquadratic filter is shown in Fig. 1. The circuit with three input terminals and one output terminal comprises one DDCC, two grounded capacitors and two resistors. The output current can be expressed as:

$$I_{out} = \frac{s^2 C_1 C_2 I_{in3} - sC_2 G_1 I_{in2} + (sC_1 G_2 - sC_1 G_1 + G_1 G_2) I_{in1}}{s^2 C_1 C_2 + s(C_2 G_1 + C_1 G_2 - C_1 G_1) + G_1 G_2} \quad \ldots(2)$$

From Eq. (2), we can see that:

(1) If $I_{in1} = I_{in2} = 0$ (opened), then I_{in3} = input current signal, a highpass filter can be obtained with I_{out}/I_{in3}.

(2) If $I_{in1} = I_{in3} = 0$ (opened), then I_{in2} = input current signal, a bandpass filter can be obtained with I_{out}/I_{in2}.

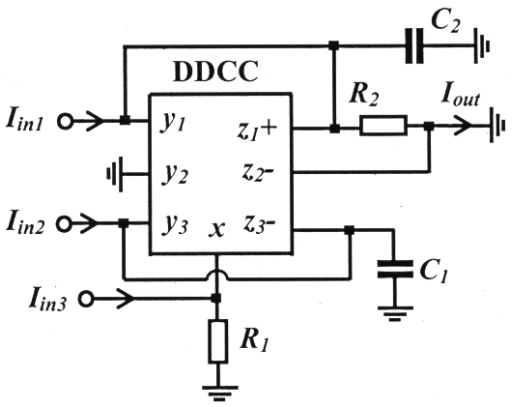

Fig. 1 — Proposed universal filter

Table 1 — Comparisons of some current-mode multi-inputs biquads

Ref.	No. of active devices	No. of passive elements	Matching constraints	Low input impedance	High output impedance
[4]	5 CCIIs	6R/2C	yes	no	yes
[5]	4 CCs	2R/2C	no	no	yes
[6]	5 CCII+s	4R/2C	yes	no	yes
[7]	4 CCIIs	4R/2C	yes	no	yes
[8]	3 CCIIs	2R/2C	no	no	yes
[9]	2 CCIIs, 1 CCIII	2R/2C	no	no	yes
[10]	3 CCIIs	3R/2C	no	no	yes
[11]	1 CCII, 1 CCIII	2R/2C	no	no	yes
[12]	2 CCIIs	3R/2C	yes	no	no
[13]	3 ICCIIs	2R/2C	no	no	yes
[14], Fig. 3	3 CCIIs	3R/2C	no	no	yes
[14], Fig. 4	3 CCIIs	2R/2C	no	no	yes
[14], Fig. 5	3 CCIIs	3R/2C	yes	no	yes
[15], Fig. 3b	1 FDCCII	2R/2C	no	no	yes
The proposed	1 DDCC	2R/2C	yes	no	no

(3) If $I_{in2} = I_{in3} = 0$ (opened) and $G_2 = G_1$, then I_{in1} = input current signal, a lowpass filter can be obtained with I_{out}/I_{in1}.
(4) If $I_{in2} = 0$ (opened) and $G_2 = G_1$, then $I_{in1} = I_{in3} = I_{in}$ = input current signal, a notch filter can be obtained with I_{out}/I_{in}.
(5) If $G_2 = G_1$, then $I_{in1} = I_{in2} = I_{in3} = I_{in}$ = input current signal, an allpass filter can be obtained with I_{out}/I_{in}.

The resonance angular frequency ω_o and the quality factor Q are given by:

$$\omega_o = \sqrt{\frac{G_1G_2}{C_1C_2}} \qquad \ldots(3)$$

and

$$Q = \frac{\sqrt{C_1C_2G_1G_2}}{C_2G_1 + C_1G_2 - C_1G_1} \qquad \ldots(4)$$

Thus, all the standard filter functions (highpass, bandpass, lowpass, notch, and allpass) can be obtained from the proposed circuit in Fig. 1. The proposed circuit uses only grounded capacitors, which are attractive for integrated circuit implementation[2,3]. Since the output impedance of the proposed circuit is not high, another current follower may be needed in order to connect the output current signal to the next stage.

The input impedances of the three input terminals are:

$$Z_{in1} = \frac{sC_1 + G_1}{s^2C_1C_2 + s(C_2G_1 + C_1G_2 - C_1G_1) + G_1G_2} \qquad \ldots(5)$$

$$Z_{in2} = \frac{sC_2 + G_2 - G_1}{s^2C_1C_2 + s(C_2G_1 + C_1G_2 - C_1G_1) + G_1G_2} \qquad \ldots(6)$$

$$Z_{in3} = \frac{sC_2 - sC_1 + G_2}{s^2C_1C_2 + s(C_2G_1 + C_1G_2 - C_1G_1) + G_1G_2} \qquad \ldots(7)$$

From Eqs (5)-(7), we can see that for high frequencies, all impedances approach zero. For low frequencies, the impedance of Z_{in1} is R_2, the impedance of Z_{in2} is (R_1-R_2), the impedance of Z_{in3} is R_1. Moreover, Z_{in1} shows a resonance effect with peak value $\frac{C_1}{C_2G_1 + C_1G_2 - C_1G_1}$, $\frac{C_2}{C_2G_1 + C_1G_2 - C_1G_1}$ for Z_{in2}, and $\frac{C_2 - C_1}{C_2G_1 + C_1G_2 - C_1G_1}$ for Z_{in3}.

3 Analysis of Sensitivities

Taking the non-idealities of the DDCC into account, the relationship of the terminal voltages and currents of DDCC can be rewritten as:

$$\begin{bmatrix} i_{y1} \\ i_{y2} \\ i_{y3} \\ v_x \\ i_{zk} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ \alpha_1(s) & -\alpha_2(s) & \alpha_3(s) & 0 & 0 \\ 0 & 0 & 0 & \pm\beta_k(s) & 0 \end{bmatrix} \begin{bmatrix} v_{y1} \\ v_{y2} \\ v_{y3} \\ i_x \\ v_{zk} \end{bmatrix} \qquad \ldots(8)$$

where $\alpha_k(s)$ represents the frequency transfer function of the internal voltage follower and $\beta_k(s)$ represent the frequency transfer function of the internal current follower of the DDCC. They can be approximated by first order lowpass functions, which can be considered to have a unity value for frequencies much lower than their corner frequencies[17]. If the circuit is working at frequencies much lower than the corner frequencies of $\alpha_k(s)$ and $\beta_k(s)$, then $\alpha_k(s) = \alpha_k = 1 - \varepsilon_{kv}$ and ε_{kv} ($|\varepsilon_{kv}| << 1$) denotes the voltage tracking error from y_k terminal to x terminal of the DDCC and $\beta_k(s) = \beta_k = 1 - \varepsilon_{ki}$ and ε_{ki} ($|\varepsilon_{kv}| << 1$) denotes the current tracking error from the x terminal to z_k terminal of the DDCC. The denominator of the non-ideal output current function for Fig. 1 becomes:

$$D(s) = s^2C_1C_2 + s(C_2G_1\alpha_3\beta_3 + C_1G_2 - C_1G_1\alpha_1\beta_1) + G_1G_2\alpha_3\beta_3 \qquad \ldots(9)$$

The resonance angular frequency ω_o and quality factor Q become:

$$\omega_o = \sqrt{\frac{G_1G_2\alpha_3\beta_3}{C_1C_2}} \qquad \ldots(10)$$

$$Q = \frac{\sqrt{C_1C_2G_1G_2\alpha_3\beta_3}}{C_2G_1\alpha_3\beta_3 + C_1G_2 - C_1G_1\alpha_1\beta_1} \qquad \ldots(11)$$

The active and passive sensitivities of ω_o and Q are shown as:

$$S^{\omega_o}_{G_1,G_2,\alpha_3,\beta_3} = -S^{\omega_o}_{C_1,C_2} = \frac{1}{2}$$

$$S_{C_1}^{Q} \cong \frac{C_1G_1 + C_2G_1 - C_1G_2}{2(C_2G_1 + C_1G_2 - C_1G_1)}$$

$$S_{C_2}^{Q} \cong \frac{C_1G_2 - C_1G_1 - C_2G_1}{2(C_2G_1 + C_1G_2 - C_1G_1)}$$

$$S_{G_1}^{Q} \cong \frac{C_1G_1 + C_1G_2 - C_2G_1}{2(C_2G_1 + C_1G_2 - C_1G_1)}$$

$$S_{G_2}^{Q} \cong \frac{C_2G_1 - C_1G_1 - C_1G_2}{2(C_2G_1 + C_1G_2 - C_1G_1)}$$

$$S_{\alpha_1,\beta_1}^{Q} \cong \frac{C_1G_1}{C_2G_1 + C_1G_2 - C_1G_1}$$

$$S_{\alpha_3,\beta_3}^{Q} \cong \frac{C_1G_2 - C_1G_1 - C_2G_1}{2(C_2G_1 + C_1G_2 - C_1G_1)}$$

4 Effect of Parasitic Elements

A non-ideal non-inverting type DDCC model[18] is shown in Fig. 2. It is shown that the real DDCC has parasitic resistors and capacitors from the y_1, y_2, y_3 and z_k terminals to the ground, and also, a series resistor at the input terminal x. Taking into account the non-ideal DDCC and assuming the circuit is working at frequencies much lower than the corner frequencies of $\alpha_k(s)$ and $\beta_k(s)$, namely, $\alpha_k \cong \beta_k \cong 1$. Moreover, in practical DDCC, the external resistors can be chosen to be much smaller than the parasitic resistors at the y and z terminals of DDCC and much greater than the parasitic resistor at the x terminal of DDCC, i.e. R_y, R_z >> R_k >> R_x. The external capacitances C_1 and C_2 can be chosen to be much greater than the parasitic capacitors at the y and z terminals of DDCC, i.e. C_y, C_z << C_1, C_2. Under these conditions, the output current of Fig. 1 becomes:

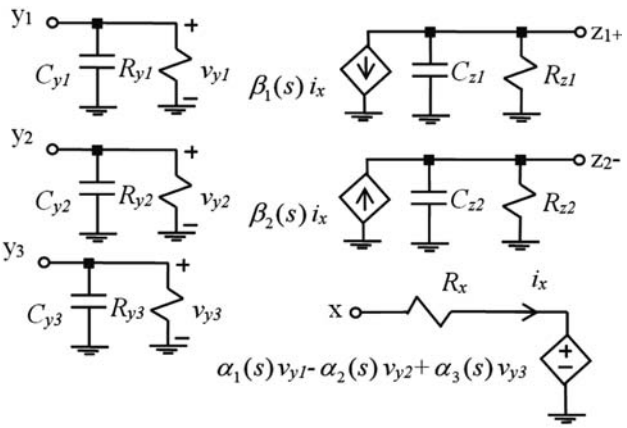

Fig. 2 — Non-ideal DDCC model

$$I_{out} \cong \frac{\begin{array}{l}[s^2C'_1C'_2 + s(C'_2G_a + C'_1G'_2 - C'_1G_2) \\ +G'_2G_a - G_2G_a]I_{in3} \\ -(sC'_2G_1 + G_1G'_2 - G_1G_2)I_{in2} \\ +(sC'_1G_2 - sC'_1G_1 + G_1G_2)I_{in1}\end{array}}{\begin{array}{l}s^2C'_1C'_2 + s(C'_2G_1 + C'_1G'_2 - C'_1G_1) \\ +G_1G'_2\end{array}} \quad \ldots(12)$$

where $C'_1 = C_1 + C_{y3} + C_{z3}$, $C'_2 = C_2 + C_{y1} + C_{z1}$, $G'_2 = G_2 + G_{y1} + G_{z1}$, $G_a = G_{y3} + G_{z3}$.

In Eq. (12), undesirable factors are yielded by the non-idealities of the DDCC. The conductances G_{y1}, G_{z1} and G_a become non-negligible at very low frequencies. To minimize the effects of the DDCC's non-idealities, the operation angular frequency should be restricted to the following conditions:

$$\omega >> \max\left\{\frac{C'_2G_a + C'_1G'_2 - C'_1G_2}{C'_1C'_2}, \sqrt{\frac{G'_2G_a - G_2G_a}{C'_1C'_2}}, \frac{G_1G'_2 - G_1G_2}{C'_2G_1}\right\} \quad \ldots(13)$$

$$\omega << \frac{G_1G_2}{C'_1(G_2 - G_1)} \quad \ldots(14)$$

5 Simulation Results

HSPICE simulations were carried out to demonstrate the feasibility of the proposed circuit in Fig. 1 using 0.18 μm, level 49 MOSFET from TSMC. The DDCC was realized by the CMOS implementation[17] in Fig. 3. The dimensions of the NMOS transistors in the DDCC are set to be W = 4.5 μm and L = 0.9 μm. The dimensions of the PMOS transistors in the DDCC are set to be W = 9 μm and L = 0.9 μm. The supply voltages are $V+$ = +0.9 V, $V-$ = –0.9 V, V_{b1} = –0.38 V and V_{b2} = 0.28 V. Figure 4 shows the simulated frequency responses for the highpass filter of Fig. 1 designed with $I_{in3} = I_{in}$, $I_{in1} = I_{in2}$ = 0, $C_1 = C_2$ = 10 pF, R_1 = 10 kΩ and R_2 = 10 kΩ. Figure 5 shows the simulated frequency responses for the bandpass filter of Fig. 1 designed with $I_{in2} = I_{in}$, $I_{in1} = I_{in3} = 0$,

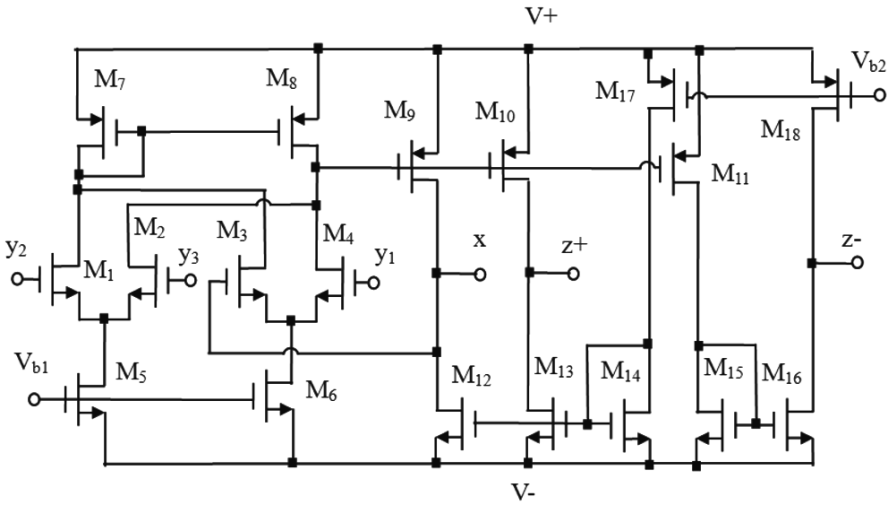

Fig. 3 — CMOS realization of the DDCC

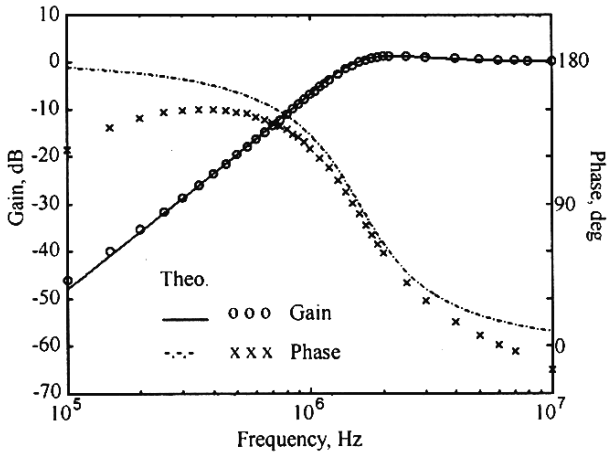

Fig. 4 — Comparisons between the theoretical and simulated results for the highpass filter in Fig. 1

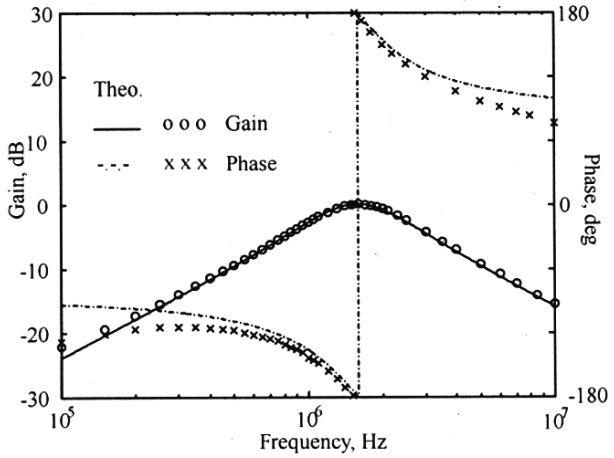

Fig. 5 — Comparisons between the theoretical and simulated results for the bandpass filter in Fig. 1

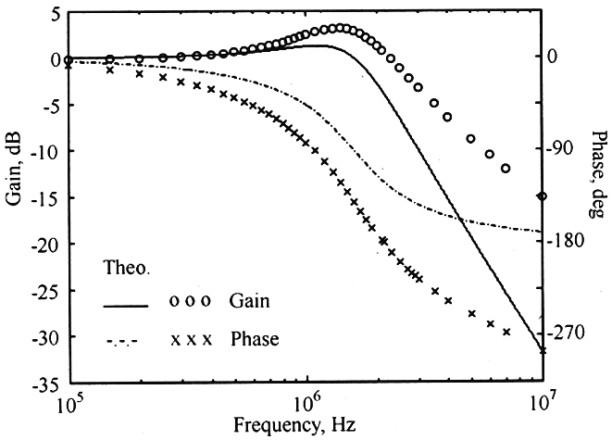

Fig. 6 — Comparisons between the theoretical and simulated results for the lowpass filter in Fig. 1

$C_1 = C_2 = 10$ pF, $R_1 = 10\ k\Omega$ and $R_2 = 10\ k\Omega$. Figure 6 shows the simulated frequency responses for the lowpass filter of Fig. 1 designed with $I_{in1} = I_{in}$, $I_{in2} = I_{in3} = 0$, $C_1 = C_2 = 10$ pF, $R_1 = 10\ k\Omega$ and $R_2 = 10\ k\Omega$. Figure 7 shows the simulated frequency responses for the notch filter of Fig. 1 designed with $I_{in1} = I_{in3} = I_{in}$, $I_{in2} = 0$, $C_1 = C_2 = 10$ pF, $R_1 = 10\ k\Omega$ and $R_2 = 10\ k\Omega$. Figure 8 shows the simulated frequency responses for the allpass filter of Fig. 1 designed with $I_{in1} = I_{in2} = I_{in3} = I_{in}$, $C_1 = C_2 = 10$ pF, $R_1 = 10\ k\Omega$ and $R_2 = 10\ k\Omega$. If all input currents are opened, the power dissipation is 159.887 μW. The lowpass filter requires resistances matching conditions. When the parasitic elements of the DDCC are taking into account, it may introduce zero at high frequency from Eq. (12). This can explain why Fig. 6

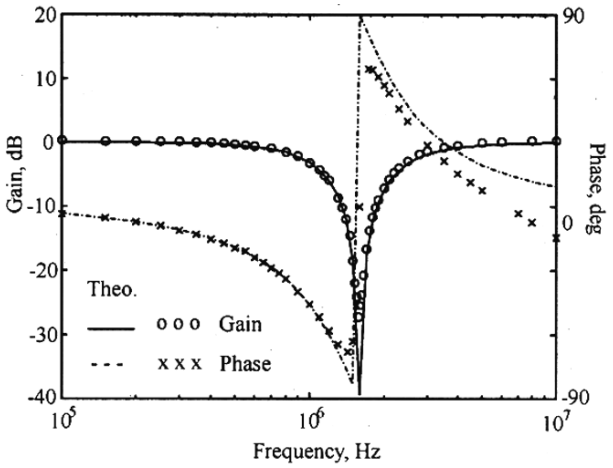

Fig. 7 — Comparisons between the theoretical and simulated results for the notch filter in Fig. 1

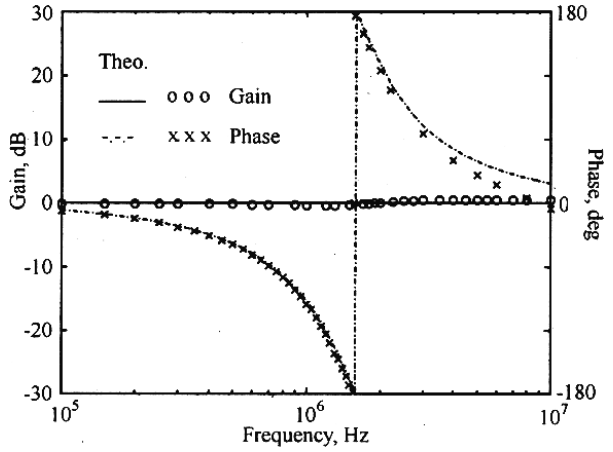

Fig. 8 — Comparisons between the theoretical and simulated results for the allpass filter in Fig. 1

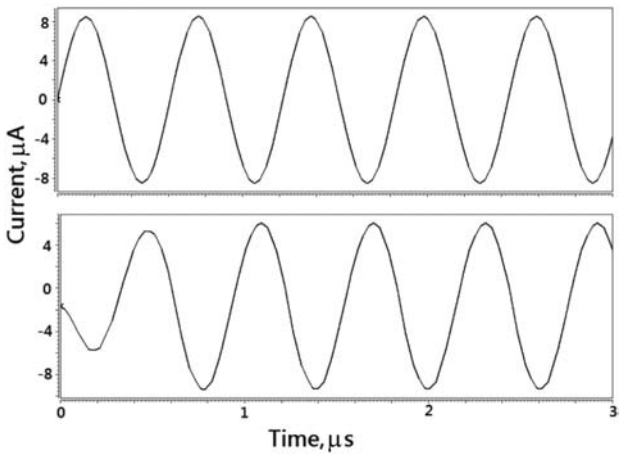

Fig. 9 — Time domain input (upper signal) and output signal waveforms to demonstrate the dynamic range of the bandpass filter in Fig. 1

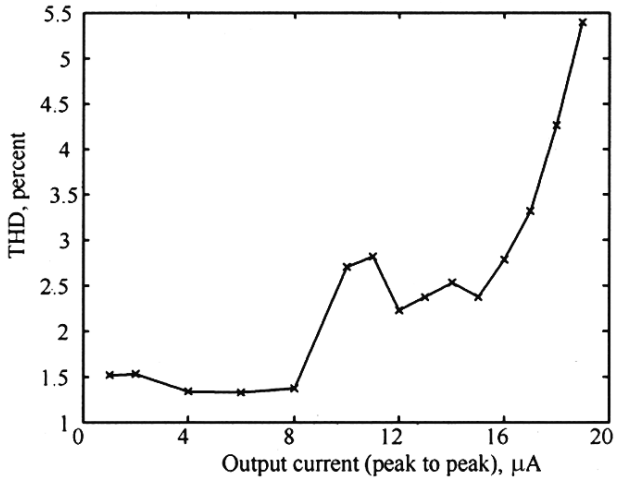

Fig. 10 — THD analysis results of the proposed bandpass filter

has non-ideal responses at high frequencies. To reduce the effect of this zero, more accurate DDCC CMOS circuits maybe required for this circuit in lowpass filter applications.

Figure 9 shows the input and output signals of bandpass response designed with I_{in2} = input current signal, $I_{in1} = I_{in3} = 0$ (opened) and $Q = 1$: $C_1 = C_2 = 10$ pF, $R_1 = 10\ k\Omega$ and $R_2 = 10\ k\Omega$. It is observed that 1.6423 MHz with 17 μAp-p input current signal levels are possible without significant distortion. In Fig. 10, total harmonic distortion (THD) of the bandpass signals are given at 1.6423 MHz operation frequency.

6 Conclusions

Several current-mode multi-inputs universal biquadratic filters were proposed in the literature[4-14]. However, the active components constructed in these biquads were not minimum. A current-mode three inputs biquad was proposed[15]. However, it employs a very complicated device (FDCCII).

In this paper, a new universal biquadratic current filter with three inputs and single output using only one DDCC, two grounded capacitors and two resistors is presented. The proposed circuit can synthesize any type of filter transfer functions. The proposed circuit employs less active elements with respect to the previous filters[4-14]. The proposed circuit employs simpler active device (DDCC) with respect to the previous biquad[15].

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