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Flipped voltage follower based low noise amplifier with 640 MHz BW at 2.26 GHz, 1.3 dB NF, 1.2V V_{dd}, and up to 10 dBm IIP3

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The design, implementation and characterization of four Low Noise Amplifier architectures in a double poly, four metal layers, 0.35 µm CMOS technology from AMS AG biased at 1.2 V with a power consumption as low as 2.73 mW operating in a frequency band ranging from 1.94 to 2.58 GHz with Noise Figure around 1.3 dB and input intercept point up to 10 dBm are presented. With the performance exhibited by the proposed topologies, it is demonstrated that the use of the Flipped Voltage Follower structure is feasible to realize amplifiers at radio frequencies with low noise figure and good linearity performance preserving its characteristic low power consumption.

Keywords: Low noise amplifier, Flipped voltage follower, Radio frequency

1 Introduction

In conventional receivers (RXs) operating in Radio Frequency (RF), the Low Noise Amplifier (LNA) is the first active stage afterwards the antenna. Its main function is to alleviate the noise added up in the communication channel in order to keep as low as possible the noise flowing in the RX chain. Moreover, it has to provide enough gain to make the signal easier to be processed by the subsequent stages. Altogether, the LNA design is a challenge due to its stringent requirements, which include[1]: moderate gain (~15 dB); low noise figure (NF ~2 dB), linearity (IIP_3~-10 d Bm), input and output impedance (50Ω) and stability factor (>1). The design efforts have been made to *RF* circuits to obtain high performance with low manufacturing costs. This trend has lead to an intense research of LNA topologies in CMOS technology[2-6]. One of the salient features of modern sub-micrometric CMOS processes is the fact that circuits realized in such technologies must operate with continuously decreasing supply voltages[7]. Furthermore, low power consumption and low supply voltages are, typically, requirements of portable electronic equipment[8-10].

From the diverse proposed techniques to reduce supply voltage requirements in mixed-signals circuits[11-13], the Flipped Voltage Follower (FVF) has been demonstrated to be a useful cell in many low-voltage/low-power systems[14-16]. Thus, three FVF based LNA architectures in 0.35 µm CMOS standard technology operating at 1.2 V voltage supply with a power consumption of 2.73mW and tuned between 1.94 and 2.58 GHz are introduced in this paper.

2 Flipped Voltage Follower LNAs

Figure 1 shows the circuit diagrams of the implemented low noise amplifier (LNAs). The FVF based architectures are the (a), (b), and (c) cases whereas the (d) case is the typical LNA topology[17]. For all the amplifiers, the bias circuit is compound by the diode connected transistor (M3 of Fig 1(a) and (b), M5 of Fig. 1(c), and M2 of Fig. 1(d), whose width is a small fraction of M1 in order to minimize its power consumption, along with resistors R2 and R3 [R3 and R4 on Fig. 1(c)], inductor L_P and capacitor C_P, whose function is to block *dc* signal from the bias circuit. Especial care must be paid when

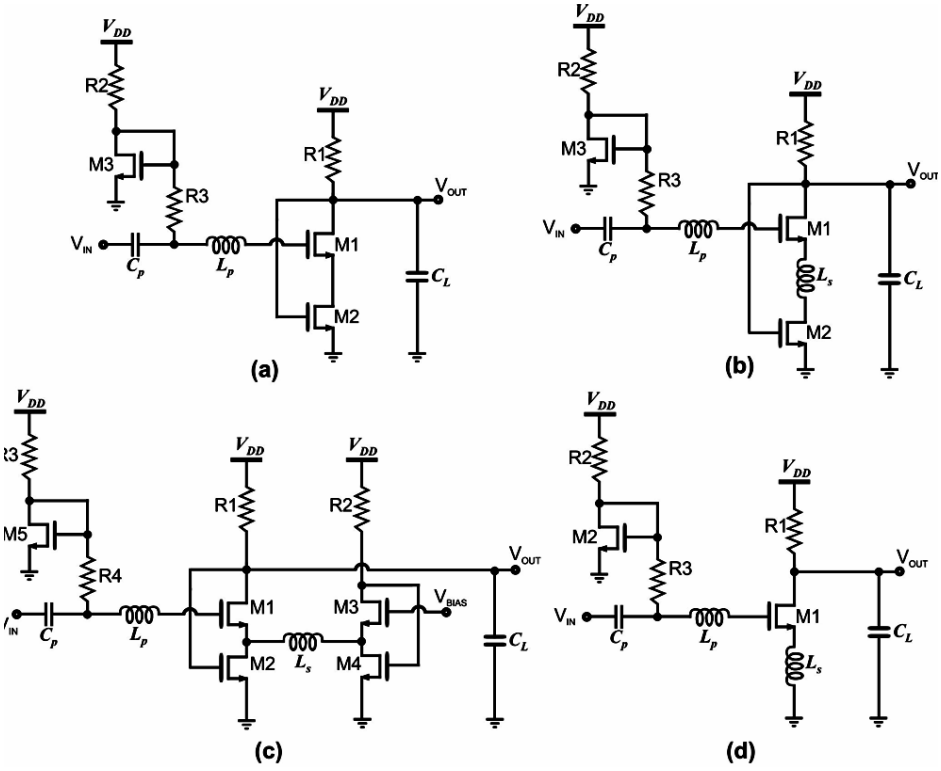

Fig. 1 — FVF based LNAs: (a) case 1; (b) case 2; (c) case 3. Typical LNA circuit: (d) case 4

choosing the value of C_P since it must have negligible reactance at the frequency at which the amplifier is tuned. On the other hand, L_P and the input parasitic capacitances of device M1, C_{gs1} and C_{gd1}, define the resonant frequency of the LNA. Furthermore, the pseudo differential LNA of Fig. 1(c) comprises two FVF joined by inductor L_S. In the drain of devices M2 and M4, there are parasitic capacitances, which resonate with L_S, performing an LNA tuning mechanism controlled by the bias current of each FVF block[18].

By realizing the input impedance analysis of the four LNA circuits, the following equations are obtained:

Case 1

$$Z_{IN} = \frac{1}{g_{d2}} + j\omega\left(L_p - \frac{g_{m1}}{C_{gs1}g_{d2}} + \frac{1}{C_{gs1}} \right) \quad \ldots(1)$$

where ω is the frequency in radians; g_{m1}, C_{gs1}, and g_{d2} are the transconductance, the parasitic capacitance between the gate and source ports, and the output conductance of devices M1 and M2 in Fig. 1(a), respectively.

Case 2

$$Z_{IN} = \frac{g_{m1}g_{d2}L_s + C_{gs1}}{C_{gs1}g_{d2}} + j\omega\left(L_s + L_g - \frac{g_{m1} + g_{d2}}{C_{gs1}g_{d2}} \right) \quad \ldots(2)$$

where also g_{m1}, C_{gs1}, and g_{d2} are the transconductance, the parasitic capacitance between the gate and source ports, and the output conductance of devices M1 and M2, as shown in Fig. 1(b), respectively.

Case 3

$$Z_{IN} = \frac{(g_{d2}+g_{d3})\left[(g_{d2}+g_{m1})\frac{(g_{d3}L_S)}{C_{gs1}} \right]}{(g_{d2}+g_{d3})^2 + \omega^2(L_S g_{d2} 2g_{d3})^2} + \frac{(g_{d2}+g_{d3})(1+\omega^2 g_{d2}g_{d3}L_g)}{(g_{d2}+g_{d3})^2 + \omega^2(L_S g_{d2}g_{d3})^2} + \frac{\omega^2 g_{d2}g_{d3}L_g(g_{d2}+g_{d3})}{(g_{d2}+g_{d3})^2 + \omega^2(L_S g_{d2}g_{d3})^2} + \frac{\omega^2 g_{d2}{g_{d3}}^2(L_g+L_S) + \omega^2 g_{d2}^2 g_{d3}L_g}{(g_{d2}+g_{d3})^2 + \omega^2(L_S g_{d2}g_{d3})^2}$$

$$+j\frac{\frac{(g_{m1}+g_{d2}+g_{d3})}{\omega C_{gs1}}(\omega L_s g_{d2} g_{d3})}{(g_{d2}+g_{d3})^2+\omega^2(L_S g_{d2} g_{d3})^2}$$
$$+j\frac{\frac{(g_{m1}+g_{d2}+g_{d3})}{\omega C_{gs1}}(g_{d2}+g_{d3})}{(g_{d2}+g_{d3})^2+\omega^2(L_S g_{d2} g_{d3})^2}$$
$$-j\omega\frac{\frac{g_{d3}^2 L_s^2 g_{d2}^2}{C_{gs1}}(g_{d2}+g_{m1})}{(g_{d2}+g_{d3})^2+\omega^2(L_S g_{d2} g_{d3})^2}$$
$$+j\omega\frac{L_s g_{d2} g_{d3}}{(g_{d2}+g_{d3})^2+\omega^2(L_S g_{d2} g_{d3})^2}$$
$$+j\omega\frac{(g_{d2}+g_{d3})[(L_g+L_S)g_{d3}+g_{d2}L_g]}{(g_{d2}+g_{d3})^2+\omega^2(L_S g_{d2} g_{d3})^2}$$
$$+j\omega\frac{\omega^2(L_S g_{d2} g_{d3})^2 L_g}{(g_{d2}+g_{d3})^2+\omega^2(L_S g_{d2} g_{d3})^2} \quad \ldots(3)$$

In this case, g_{m1}, C_{gs1}, g_{d2} and g_{d3} are the transconductance, the parasitic capacitance between the gate and source ports, and the output conductances of devices M1, M2 and M3 from Fig. 1(c), respectively.

and Case 4

$$Z_{IN}=\frac{g_{m1}L_s}{C_{gs1}}+j\omega\left(L_s+L_g-\frac{1}{\omega C_{gs1}}\right) \quad \ldots(4)$$

where g_{m1} and C_{gs1} are the transconductance and parasitic capacitance between the gate and source ports of transistor M1 from Fig. 1(d), respectively.

By inspection of expressions given in Eqs (1) to (4), it can be appreciated that the real part of the input impedances in cases 1 and 2 are: inversely dependent on the conductance between the drain and source ports of transistor M2 and to some extent, proportional to L_s, respectively. The real part of the impedance in Case 3 is determined by many more parameters. Finally, the real part of the input impedance in the amplifier in case 4 is proportional to the ratio between the product of the transconductance of M1 by L_s and C_{gs1}.

On the other hand, to determine the values of the elements of the LNA, it is assumed a frequency of operation of 2 GHz, which is given by the Federal Communications Commission (FCC) for the Advanced Wireless Services[19] H Block (AWSH-B) and a real input impedance of 50 Ω. The bias current in every LNA was established to be 2 mA.

2.1 Noise behaviour of the FVF LNAs

Taking into account the small signal noise model[17] of the MOS as shown in Fig. 2, the noise current in the drain terminal of the transistor is expressed as:

$$\overline{i_{nd}^2}=4kT\gamma g_{d0}\Delta f \quad \ldots(5)$$

where k is Boltzmann constant (1.38×10^{-23} J/K), T the absolute temperature (in kelvin), g_{d0} the drain-source conductance at $V_{DS}=0$ and Δf is the bandwidth of the noise (in hertz). The g_{d0} parameter has a unitary value at $V_{DS}=0$. Typically, the body effect coefficient, γ, has a value between 2 and 3. On the other hand, a minimum NF can be attained by considering:

$$NF_{\min}=1+\frac{2}{\sqrt{5}}\frac{\omega}{\omega_T}\sqrt{\gamma\delta\left(1-|c|^2\right)} \quad \ldots(6)$$

where ω and ω_T are the resonant frequency and cut-off frequency of the LNA, respectively, and are expressed as:

$$\omega=\frac{1}{\sqrt{L_p C_{gs1}}} \quad \ldots(7)$$

$$\omega_T=\frac{g_{m1}}{C_{gs1}} \quad \ldots(8)$$

and c is the correlation coefficient of the noise between the gate and drain ports of the transistor, whose theoretical value[20] is 0.395.

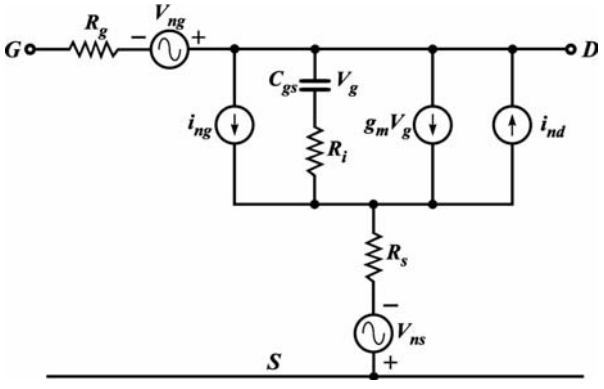

Fig. 2 — Small signal noise model of the MOS

Additionally, the most commonly accepted definition of the NF is:

$$NF = \frac{SNR_{\text{IN}}}{SNR_{\text{OUT}}} \quad \ldots(9)$$

where SNR_{IN} and SNR_{OUT} are the signal-to-noise ratio measured at the input and output ports, respectively. NF is a measure of how much the *SNR* is degraded when a signal passes through a system.

2.2 Linearity performance of the FVF LNAs

In addition to the NF, gain and input matching, the LNA design must consider the linearity. The most commonly used metric to determine the distortion produced by a circuit is the third order intercept point, IIP3, which can be obtained by means of the two-tone test (two input signals at frequencies ω_1 and ω_2 are fed to the LNA), and expressed [1] as :

$$IIP3 = \frac{\Delta P}{2} + P_{\text{IN}} \quad \ldots(10)$$

where ΔP is the difference of power between the fundamental signal, ω_1, and the third order intermodulation component, $2\omega_1 \pm \omega_2$.

3 Experimental Results

Following the design guidelines described in the previous section, the design of the LNA structures was carried out. Table 1 presents the design details. The die photograph for each case is shown in Fig. 3.

The measurements of the LNAs were realized with a Vector Network Analyzer (VNA) whose frequency capabilities attain the 4 GHz. The use of Ground-Signal-Ground (GSG) probes and a calibration substrate (ISS Picoprobe) were necessary to realize the characterization of the circuits directly on the die.

The measured NF of the LNAs is shown in Fig. 4. It can be appreciated that around 2 GHz, the NF of the proposed amplifiers is optimum whereas the NF of the fourth amplifier is good at a lower frequency (≈1 GHz). At 2.18 GHz, the LNA case 1 presents a NF=1.4 dB; for the case 2, the LNA exhibits a NF=1.49 dB at 2.12 GHz; case 3 LNA has a NF=1.43 dB at 2.455 GHz; finally, case 4 LNA possesses a NF=1.27 dB at 1.11 GHz. These results are good for

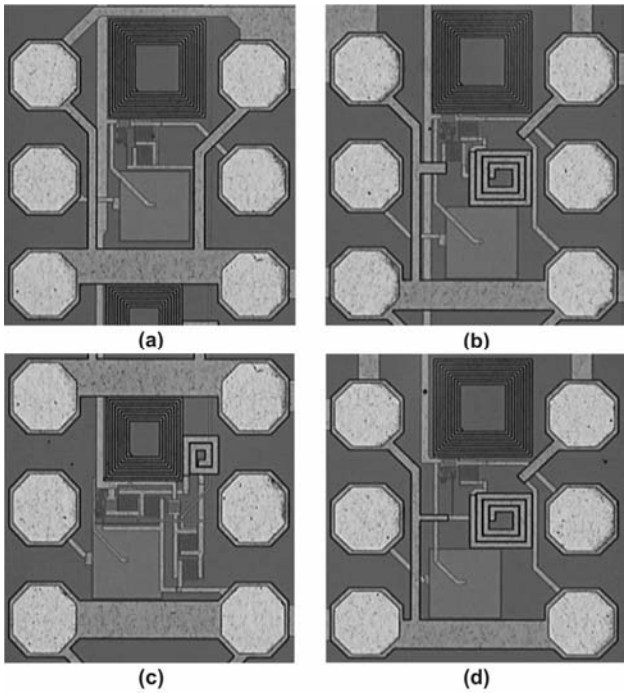

Fig. 3 — Die photograph of the LNAs: (a) Case 1, (b) Case 2, (c) Case 3 and (d) Case 4

Table 1 — Design details of the accomplished LNA structures

Element	Case 1	Case 2	Case 3	Case 4
M1	330µm / 0.35µm	330µm / 0.35µm	330µm / 0.35µm	330µm / 0.35µm
M2	330µm / 0.35µm	330µm / 0.35µm	330µm / 0.35µm	16µm / 0.35µm
M3	16µm / 0.35µm	16µm / 0.35µm	330µm / 0.35µm	-
M4	-	-	330µm / 0.35µm	-
M5	-	-	16µm / 0.35µm	-
M6	-	-	16µm / 0.35µm	-
R1	200Ω	200Ω	200Ω	200Ω
R2	2kΩ	2kΩ	200Ω	2kΩ
R3	4kΩ	4kΩ	2KΩ	4kΩ
R4			4KΩ	-
Lg	15.7nH	15.7nH	15.7nH	15.7nH
Ls	-	1nH	1nH	1nH
Cp	11pF	11pF	11pF	11pF

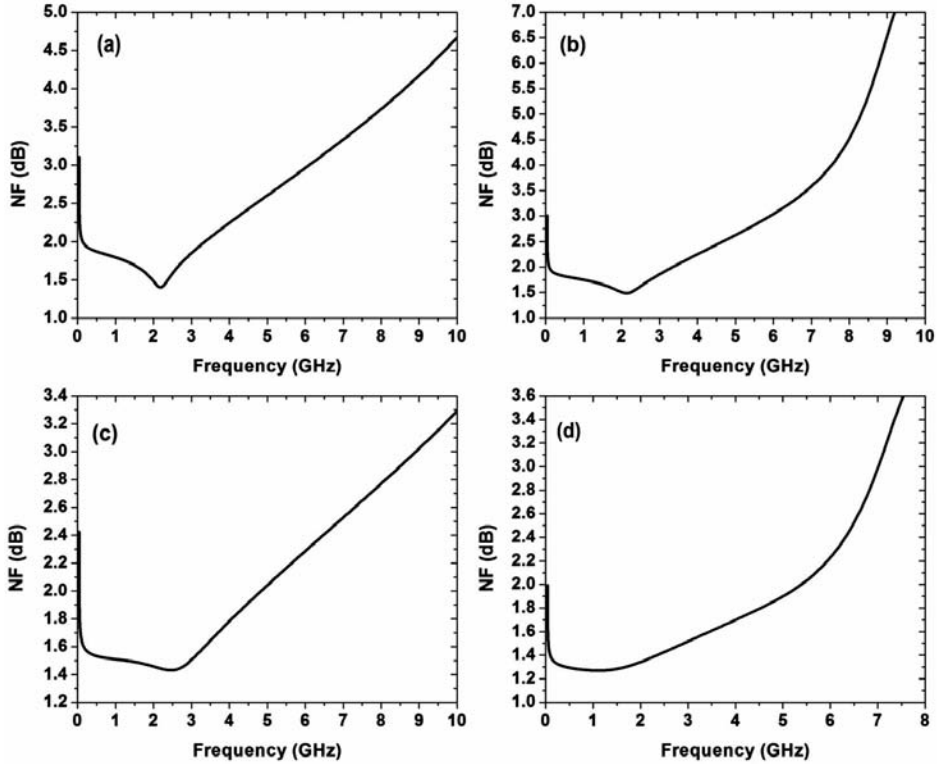

Fig. 4 — Noise Figure for LNAs proposed: (a) Case 1, (b) Case 2, (c) Case 3 and (d) Case 4

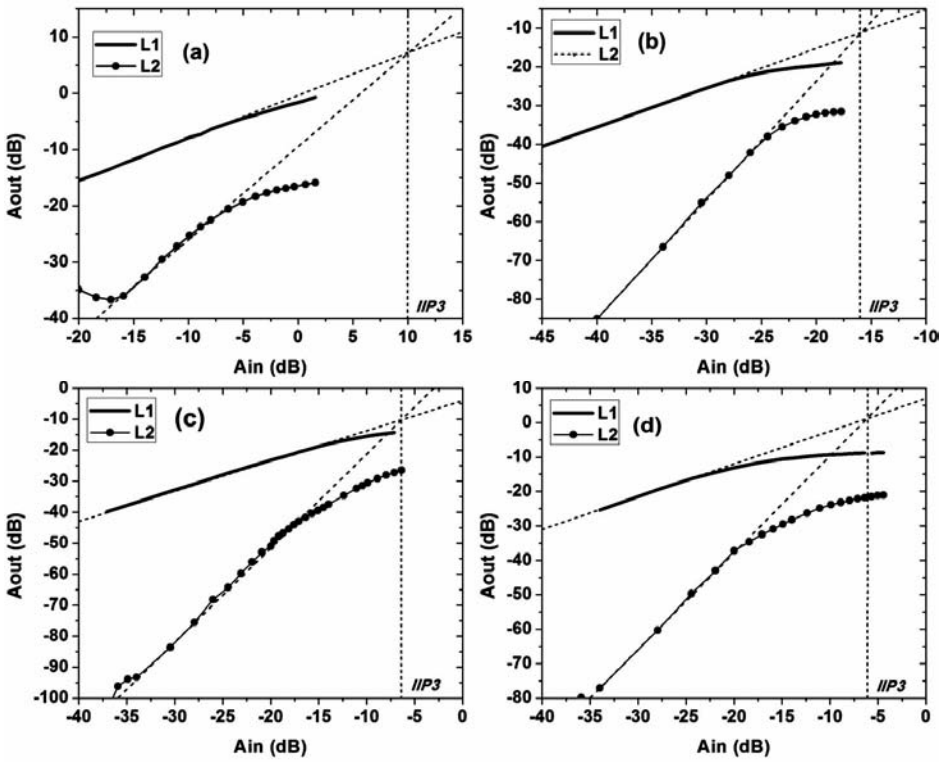

Fig. 5 — IIP3 for LNAs: (a) Case 1 (b) Case 2 (c) Case 3 (d) Case 4

Table 2 — Summary of measurement results and performance comparison

Parameter	Reference					This work			
	[2]	[3]	[5]	[21]	[22]	Case 1	Case 2	Case 3	Case 4
Technology	CMOS 90 nm	CMOS 0.25 μm	CMOS 65 nm	CMOS 0.13 μm	SiGe 0.25 μm	CMOS 0.35 μm			
Supply [V]	1.2	1.2, 1.5	1	1.2	5	1.2			
Consumption [mW]	0.68	13, 35	7	2.79	200	2.58	2.73	4.64	4.93
Frequency [GHz]	2.45	1-5.2	5.2	2.45, 6	1.92-1.98	1.94-2.58	1.93-2.37	2.01-2.58	1.53-1.94
IIP3 [dBm]	-4	≥-1.5	-6	-4.3,-5.6	+40	10	–15.8	–6.4	–6
NF [dB]	4.36	6.5-8.3	2.9-5.4	2.8, 3.8	0.9	1.4	1.49	1.43	1.27
K	NA	NA	NA	NA	NA	7.2	5.42	4.15	3.64
Δ	NA	NA	NA	NA	NA	0.083	0.11	0.11	0.025

the proposed LNAs since a NF below 2 dB is hard to achieve by integrated[1] LNAs.

To estimate the *IIP*3 of the LNAs, the two-tone test has been accomplished. Figure 5 shows the main signal (*L*1), the *IM*3 signal (third-order Intermodulation, *L*2), and their corresponding intercept point of each LNA. As can be seen, the proposed LNAs present an IIP3 of –10 dBm, –15.8 dBm, –6.4 dBm, respectively, whereas the fourth amplifier has An IIP3 of –6 dBm.

The main results achieved of these LNAs are summarized in Table 2. The proposed amplifiers exhibit low power consumption as compared to some other approaches reported in the literature[2-5,21,22], despite the technology employed for building the circuits up is far from the cutting edge of the deep-submicrometer CMOS technologies. In addition, the frequencies reached with the advised circuits are higher than some other reported[3,22], even though those were fabricated in shorter-channel CMOS technologies. Furthermore, the attained NF is below 1.5 dB, which is an important achievement since only one of the other LNAs reviewed exhibits[22] NF≤2 dB. In terms of linearity, the IIP3 achieved by the LNA case 1 is the best number of the four considered possibilities, as compared to the other amplifiers is quite competitive except for that published in Ref. 22; however, the technology employed in that case was SiGe:C with 5V power supply. Finally, the stability factor, *K*, shows that the four structures are unconditionally stable. From the results obtained, it can be seen that the case 1 LNA is the circuit that exhibits the best Figures of Merit (FOMs) regarding linearity, power consumption, Noise Figure, stability factor and frequency range.

4 Conclusions

Design and performance of four different CMOS LNA topologies in the 1.98-2.54 GHz band are reported in this work. Three of those structures, present the novelty of working at low voltage supply, 1.2 V in a double poly, four metal layers, 0.35-μm CMOS technology, and achieve a power consumption as low as 2.73 mW as well as a Noise Figure of 1.5 dB and an IIP3 of 10 dBm. Additionally, coupling with both, output and input port, around 50 Ω is exhibited by the proposed architectures.

The low voltage operation of the proposed amplifiers makes them an attractive solution for portable wireless receivers when compared to some other LNAs. The measured values of the NF for the proposed LNAs (≤ 1.5 dB) are good numbers. Such a low NF impacts positively on the subsequent stages on the receiver path.

Based on the results, it is concluded that the proposed LNAs are good candidates for being employed in modern wireless communication technologies which required low power consumption, such as those from the Personal Area Network (PAN) and Local Area Network (LAN), for instance: Bluetooth, Zigbee and WiFi to name a few.

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