Indian Journal of Pure & Applied Physics
Vol. 60, March 2022, pp. 238-245

# Performance Analysis of a High-Speed High-Precision Dynamic Comparator

Vaithiyanathan Dhandapani*, Ashish Mishra, Ankit Kumar, Alok Kumar Mishra, Sachin Singh & Baljit Kaur

Department of Electronics and Communication Engineering, National Institute of Technology Delhi, New Delhi – 110 040

*Received 9 October 2021; accepted 7 February 2022*

Comparators are the key structure of any analog-to-digital-converters (ADCs). In recent days various low power and high-speed comparators have been introduced and reported by many researchers. This paper presents an examination of various kinds of comparators which is the second most generally utilized hardware block. The preamplifier stage is mainly concerned with the power of the comparator, while latch structure defines the overall comparison speed. Hence, both the stages of dynamic comparator need to be designed efficiently for achieving optimized performance. Proper optimization of transistors in the comparator circuit helps to achieve low power dissipation and operate at a sufficiently low offset voltage. All the circuit has been implemented and simulated using cadence virtuoso tool in 180 nm technology and uses a clock of frequency 500 MHz to control the two stages of the comparator and provides rail to rail input common-mode voltage. The power and delay of different comparator circuits have been analyzed. The results obtained from the analysis show that there is a 32% reduction in power and the comparator design was 29% faster as compared to the conventional circuit.

**Keywords**: Dynamic comparator, Preamplifier, low-power analog design, high speed, low-offset, analog-to-digital-converters (ADCs)

## 1 Introduction

Nowadays most handheld devices, medical systems, communication systems use Analog to Digital converters (ADCs). With an increase in portable systems, we need devices to be battery operated and ADC shave comparator as one of the key structures and hence should be of low power, higher speed, occupying the lesser area and should be able to work efficiently on lower offset voltages. As we are going to lower technology nodes, the threshold voltage is not scaling down in proportion to technology node shrinking, hence limiting the power supply. Therefore, low-power challenges occur in high-Speed comparators. The preliminary study of reported works was implemented and performances were discussed in our earlier paper[1]. Earlier designs were using static comparators but they suffer from high power dissipation problems. As they are static and are always ON and also, they are sluggish and less stable due to the absence of a feedback path. While dynamic comparator solves this problem by utilizing a positive feedback path to improve the performance and also there is no static power consumption. Also, earlier designs involve the use of a one-stage dynamic comparator that suffers from kickback noise. Earlier designs had a problem with kickback noise which is caused due to the capacitive path formed between output and input nodes. These single-stage comparators also called single tail dynamic comparators suffer from high delay and larger dynamic power consumption. These problems are solved by using double stage dynamic comparator also called a dual tail dynamic comparator solves these problems. Moreover, these comparators efficiently reduce the power consumption and also increase the speed, and can work efficiently at lower supply voltages. In the two-stage dynamic comparators, the first stage amplifies the differential input while the second stage improves the speed. The preamplifier stage is concerned with power and the latch stage is concerned mainly with speed. Many works related to these dual tail comparators can be found in the literature. A two-stage dynamic comparator requires a clock and its inverted signal or we can use some form of control circuitry to control the two stages of the comparator and for achieving this stricter timing diagram is required. To solve this problem comparator reported in[2] uses the common-mode voltage of the output of the preamplifier stage to turn on the latch stage hence this design is having only one clock.

The comparator circuit reported in[3] is consumed lesser lower power by isolating the preamplifier circuit from the main circuitry whenever the

*Corresponding author: (E-mail: dvaithiyanathan@nitdelhi.ac.in)

preamplifier stage is not in use. The work reported in[4] is a new design to reduce the power consumption by using XOR gate as preventing operation of preamplifier stage. Besides it mainly designs techniques such as offset cancellation technique, body driven technique, self-biasing techniques, and many others has been reported to fulfill the requirements of low power, low offset, and higher speed comparator designs. Charge shared techniques are usually not preferable at lower supply voltage techniques. The reported work in[5] uses cross-coupled circuitry to enhance the preamplifier which has a huge impact on gain and also it is hasty due to the modification in the design of the latch stage. Also, in[6] design improves the offset voltage while keeping the comparator consuming a lesser area and power with a trade-off with delay.

In this paper, a conventional comparator has been implemented simulated and analyses and a performance comparison with the different reported comparators circuitry. Here low power low offset comparator designs have been studied and reported. In all the designs reported the power is saved by either cutting the preamplifier stage is cut in the reset phase or the evaluation phase just after the comparison begins. And for high-speed designs, PMOS-PMOS architecture is used in the preamplifier stage and the gain of the preamplifier stage is increased to do a faster comparison and also for amplifying the lower offset voltage signals.

This paper is organized as follows. Section 2 presents the conventional and previously reported circuits. In Section 3, performance comparison has been reported and finally concluded in Section 4.

## 2 Dynamic Comparators

### 2.1 Conventional comparator

Figure 1 presents the conventional comparator which consists of two input stages called the preamplifier stage and the decision-making stage is also known as the latch stage. Preamplifier does the pre-amplification of the applied input signals and also helps in getting rid of kickback noise problems occurring in single-stage dynamic comparators while the next stage amplifies the output of the first stage to Vdd at one side and GND at the other side. The preamplifier stage is used to achieve the minimum required pre-amplification so that the impact of the offset voltage of the latch stage on becoming negligible also helps in the prevention of noise

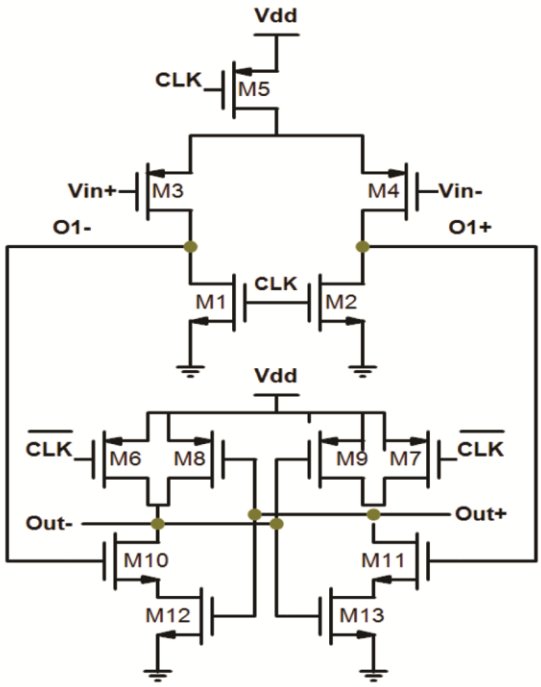


Fig. 1 — Conventional two-stage dynamic comparator.

disturbance on the total applied input voltage. The existence of back-to-back inverters creates a positive feedback path for the comparator, ensuring reliability and speeding up the comparison process. The presence of the preamplifier stage reduces the kickback noise as compared to comparators having single stages.

The size of preamplifier input transistors M3, M4 is high compared to the other transistor size. This helps in achieving a higher gain and also cancels the impact of the offset voltage. In addition, the size of the latch's input transistor is deliberately selected to meet the speed requirement. As a consequence, the latch determines the speed the most, while the pre-amplifier determines the power consumption. Large parasitic capacitors at the output nodes of the preamplifier sink a huge amount of power from Vdd. There are two phases of comparator operation are reset phase and the evaluation phase of the decision-making phase. The CLK is set to 1 during the reset process to reset the comparator's first and second stages to GND and Vdd, respectively to avoid hysteresis. Due to this M5 is turned off and the preamplifier stage is off while PMOS M6 and M7 are turned ON leading to the setting of Out+ and Out− to Vdd. Hence, transistors M12 and M13 are turned ON leading to resetting of any offset voltage present at the output of the preamplifier phase. The flow of the reset phase operation is shown in Fig. 2.

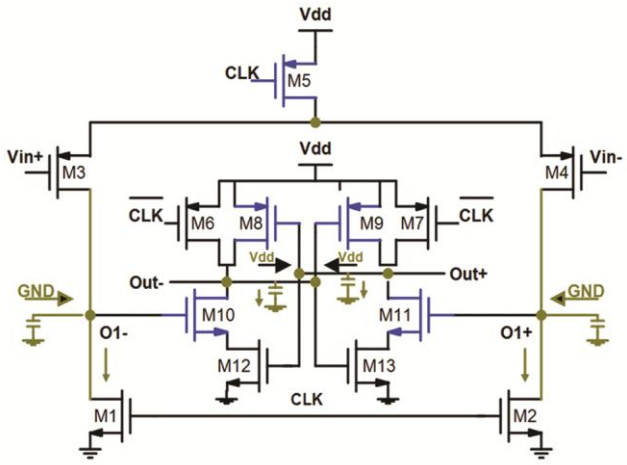


Fig. 2 — Reset phase of the conventional two-stage dynamic comparator.

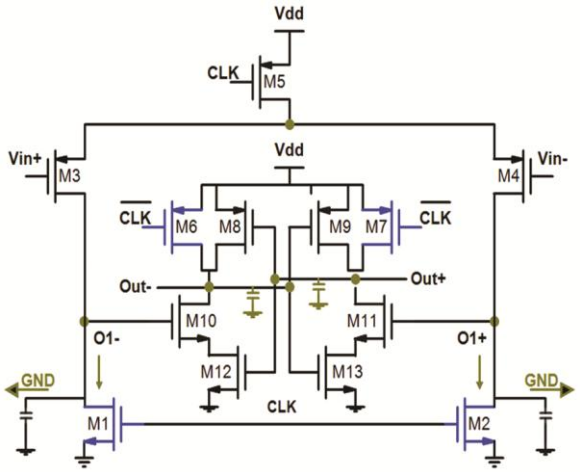


Fig. 3 — Evaluation phase of the conventional two-stage dynamic comparator.

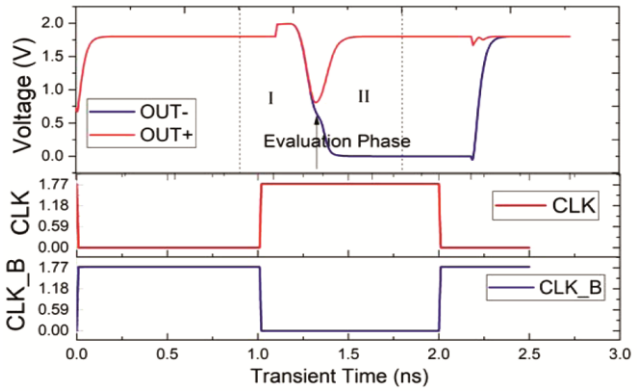


Fig. 4 — Output waveform of the conventional two-stage dynamic comparator.

The evaluation phase consists of the comparison phase and decision-making phase as shown in Fig. 3. In the second phase, when CLK is set to 0, then it marks the start of the decision-making stage. In the pre-amplification stage, parasitic capacitance appearing at the output of this stage near M10 and M11 transistors starts to charge based on changes in the input signals at M3 and M4 transistors. Here, as CLK changes to 0, M5 turns ON and the preamplifier starts working and charging of the output nodes O1+ and O1− based on the applied input signals (Vin+ − Vin−). The voltages O1+ and O1− at the input of the second stage turns on M10 and M11 transistors become greater than the threshold value of these transistors, latch gets actuated and starts the amplification process with this certain delay. Here, we found out that even after the comparison is made, the first stage consumes a huge amount of power. The excess power consumption is unavoidable as the comparison delay is non-predictable. Indeed, the comparison delay radically changes with a few variables, like Input differential voltage (Vid), common-mode voltage (Vcm), supply voltage (Vdd), and temperature. Dynamic comparators have one additional clock control circuit which helps in controlling the two stages and saving power. Due to this additional circuit, the timing waveform applied to the comparator needs to be very much stricter as it is concerned with the power of the comparator.

There is certain design constraints associated with the designing of the conventional comparator. The size of the input transistors M3 and M4 is taken larger for achieving higher preamplifier gain. In this work, the clock is set at 500MHz in all the circuits to have a better understanding of speed and power at a given clock frequency. The simulated output waveform of the conventional two-stage dynamic comparator is in Fig. 4.

### 2.2 19T Dynamic Comparator

Figure 5 represents the schematic diagram of 19 transistors (19T) dynamic comparator[7]. There are a total of 19 transistors in this circuitry compared to the conventional one which has 13 transistors (13T) hence area penalty is given for lower power. The additional increase in transistors helps in the overall reduction of power by turning off the preamplifier when it is not being used while the comparison is performed. At the same time, the speed is not affected as the latch stage is almost done finishing the comparison. As discussed in conventional design excess power consumed cannot be eliminated. This is achieved by the use of two transistors M14 and M15 which are connected to the output of the latch stage

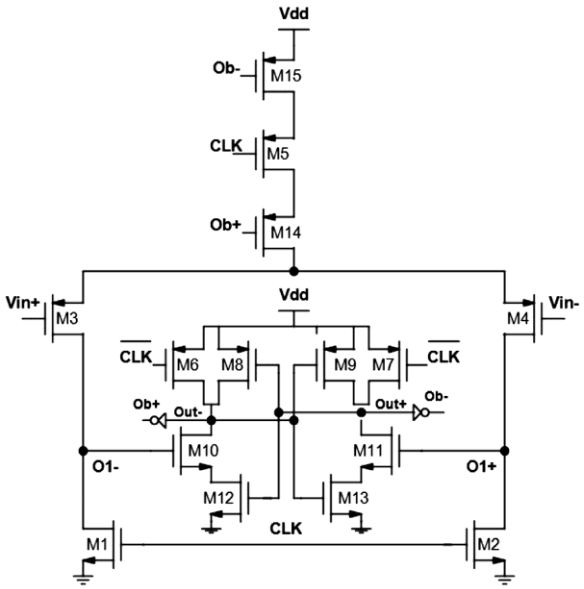


Fig. 5 — 19T Dynamic Comparator[7].

through inverters. The series arrangement of M5, M14, M15 transistors is not significant in regards to the usefulness. However, it is picked in this approach to have a layout as symmetrical. Also, the output of the latch stage is connected to the inverters because – (i) To isolate the output nodes of the latch stage from the load capacitor and (ii) It avoids latch offset voltage due to load capacitor mismatch or speed reduction due to large load capacitors.

The inverter's delay helps in achieving stability for the output of the latch stage and then immediately turns off the preamplifier stage. The circuit also has two stages, the preamplifier stage, and the latch stage, and works in two phases of operation - the reset phase and the evaluation phase. When the clock is high M5 turns off and the latch stage starts its operation and Out+ and Out− are settled to Vdd (1.8 V) due to which any voltage present at the output nodes of the preamplifier stage is settled to the ground leading to the cancellation of any offset voltage present in the circuit, called as reset phase. When the clock is low after 1ns, the transistor M5 is turned ON and the preamplifier starts working and starts charging the output nodes O1+ and O1– based on the input differential signal, and comparison is completed.

### 2.3 28T Dynamic Comparator

The dynamic comparator in Fig. 6[9] uses 28 transistors in this circuitry compared to the conventional one which has 13 transistors hence area penalty is huge, but the area penalty is minimized

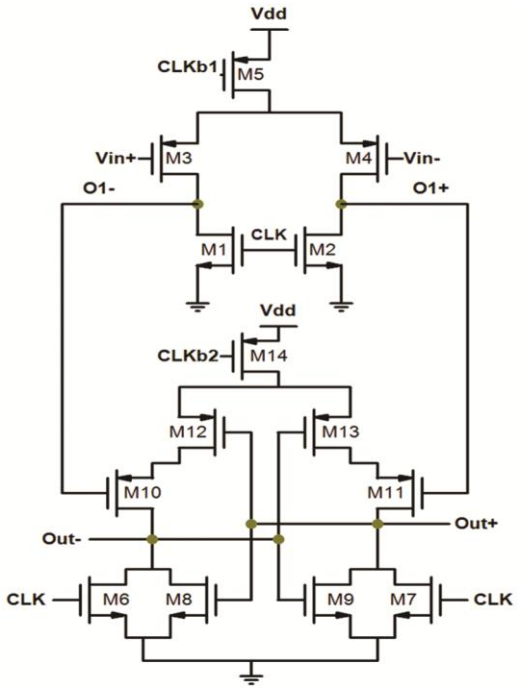


Fig. 6 — 28T Dynamic Comparator[9].

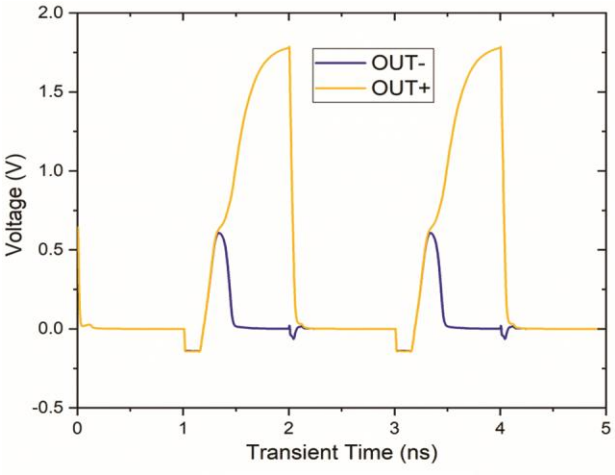


Fig. 7 — Output waveform of 28T two-stage dynamic comparator[9]

through optimization in speed. The output waveform of the 28T two-stage dynamic comparator is in Fig. 7. The use of PMOS latch makes the comparison faster by approximately 50 % as compared to the conventional.

The circuit operates in two stages the reset stage is the similar operation of a conventional circuit. The first stage enhances the applied input signals under a certain timeframe. Then the latch stage starts functioning after a certain delay associated with PMOS architecture for amplifying the applied input signals. Simultaneously, the current source M5

transistor of the first stage is turned off by the CLK when it reaches the value of 1 and helps in saving power by turning off this preamplifier stage in the evaluation phase. Also, clkb1 and clkb2 are having one circuitry whose design is very much important as shown in Fig. 8.

### 2.4 31T Dynamic Comparator

There are a total of 31 transistors used in the circuit in Fig. 9[10], compared to the conventional one having the advantage of low power, high speed, low offset, and high gain. Here, the circuit also has two stages - the preamplifier stage and the latch stage and works in two phases of operation, the reset phase, and the evaluation phase. The cross-coupled transistors formed by transistors M3, M4, M5 increase the preamplifier gain so that comparison is done very quickly, and hence speed is significantly improved. Rather than the ordinary comparator, a PMOS latch is utilized in which the decision-making stage is actuated with a predetermined delay. Also, the circuit uses PMOS-PMOS architecture in the latch stage and

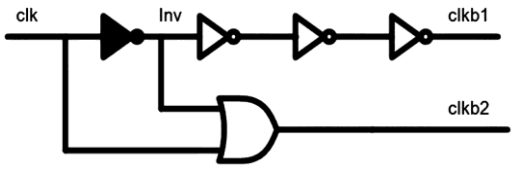


Fig. 8 — Control circuit adopted for 28T and 31T dynamic comparator[10].

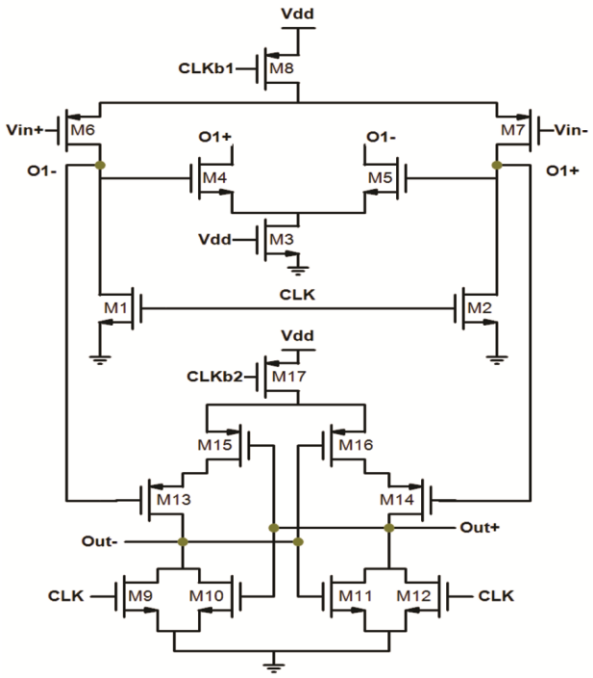


Fig. 9 — 31T Dynamic Comparator[10].

the positive feedback makes the comparator comparatively hasty.

From Fig. 10 it is observed that the output waveform is the same as that of the 28T dynamic comparator except that this circuit has higher preamplifier gain owing to higher speed as compared to the conventional one. This new design cuts the preamplifier from the latch stage and the output of O1+ and O1− does not rise to full Vdd, it's less than Vdd. Hence power is significantly reduced. This technique reduces the preamplifier stage power consumption significantly without affecting the comparison speed.

Here the control circuitry increases the transistor count and hence the die area increases. The black inverter in Fig. 8 is designed very precisely as it plays a very important role in controlling the delay of overall circuitry. Moreover, this leads to the generation of clkb1 and clkb2 which is used to control the latches and hence overall impact the delay of a comparator. When the value of clkb1 changes to High (1) as reflected from the timing waveform in Fig. 11, this turns off the transistor M8 and this transistor helps in controlling the activity of the preamplifier stage. The preamplifier gets deactivated and the only power consumed is by the transistors of the next stage, hence saving a lot of power by this technique. In the meantime, the cross-coupled circuitry proceeds with pre-amplification at no expense of power utilization. The Circuit is faster and consumes lesser power than conventional and other circuits but the area penalty is huge. The delay time, which was previously set, is now easily controllable and can be fine-tuned to its ideal value. However, in a traditional

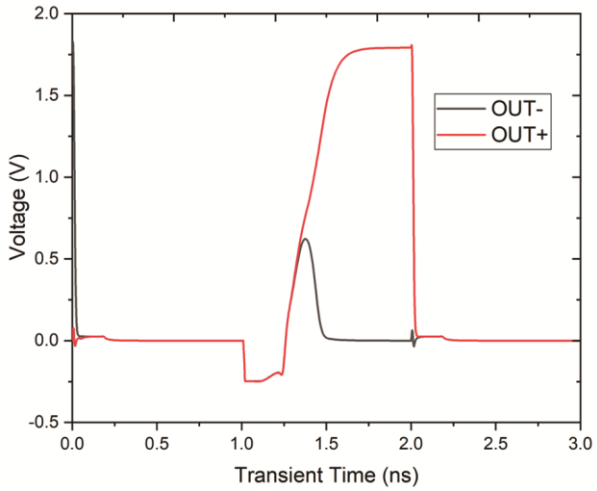


Fig. 10 — Output waveform of 31T two-stage dynamic comparator[10].

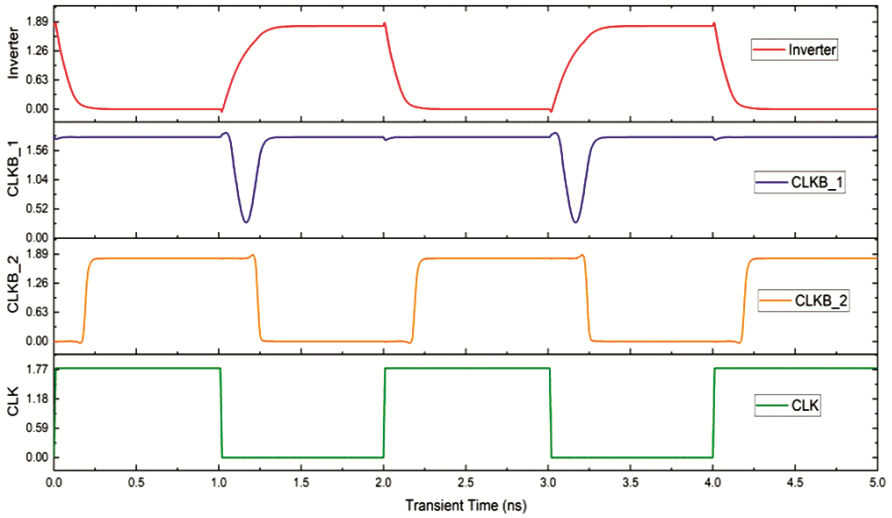


Fig. 11 — Output waveform for control circuit for 28T and 31T dynamic comparator.

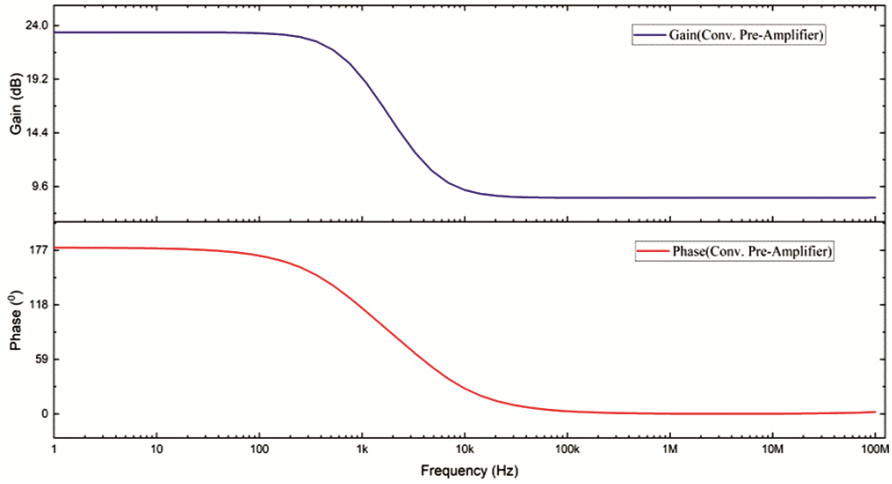


Fig. 12 — Preamplifier Gain for 13T conventional dynamic comparator.

comparator, the delay is inextricably linked to the time taken to charge the latch stage's input nodes, which was based on the NMOS architecture. This structure can also be implemented using NMOS transistors i.e. the latch and preamplifier with input NMOS transistors. This will result in a higher speed design because of the inherent superiority of NMOS transistors over PMOS transistors. In recent years there many more comparator circuits are proposed by researchers[11-18].

## 3 simulation results and comparisons

The circuits are designed and implemented in 0.18 µm CMOS technology using the cadence Virtuoso tool to achieve a dynamic offset of 2.7 mV. We have used a supply voltage of 1.8 V while simulating the various designs. Fig. 12 represents the preamplifier gain of the conventional circuit. We calculated the gain of the preamplifier stage to check the impact of the gain of the preamplifier stage on the performance of the comparator. The gain of the preamplifier stage was found to be approximately 23 dB. This ordinary comparator consumes approximately 350 µW of power and hence is very much power-hungry and is not suitable for portable systems. We also found out through the study of different dynamic comparators if we want to design a high-speed comparator the NMOS-NMOS architecture is the most preferable but at the expense of power consumption of four times as compared to the conventional one.

The gain of the 19 T dynamic comparator was found to be approximately 26 dB and is nearly two times higher. This increase in gain is due to design changes in the preamplifier stage design and hence it

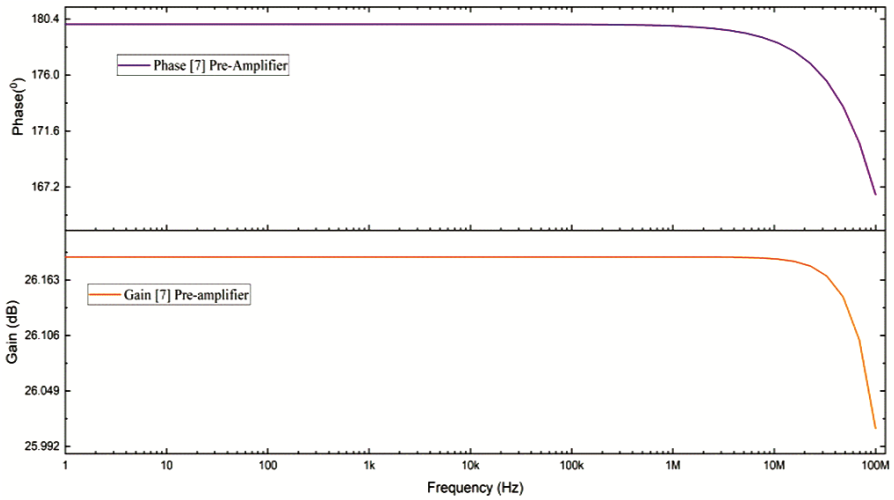


Fig. 13 — Preamplifier Gain for 19T Dynamic Comparator.

Table. 1 — Preamplifier Gain of different circuit

| Comparator Circuits | Preamplifier Gain(dB) |
|---|---|
| Conventional circuit | 23 |
| [7] | 26 |

Table. 2 — Comparison of power and delay of various comparators

| Comparator Circuits | Power (µW) | Delay (ps) | power change (%) | Delay change (%) |
|---|---|---|---|---|
| Conventional | 345.43 | 294.13 | -- | -- |
| [7] | 210.34 | 224 | 39.10 | 23.84 |
| [9] | 256.72 | 156.03 | 25.63 | 46.95 |
| [10] | 235.60 | 210.58 | 31.79 | 28.40 |

can even amplify the low offer voltage to a greater value and it becomes easy for the second stage to make a decision and comparison speed is increased. This 19T comparator is approximately 25 % faster as compared to the conventional one. So, preamplifier gain is one of the important factors on which comparator speed depends. We can further increase these gain values by properly optimizing the circuit for a faster comparison. Fig. 12 represents the preamplifier gain of the 19T dynamic comparator. And by the use of proper control circuit design, we can control the power and also the area of the circuit.

Tables 1 and 2 presented the comparison of conventional and various reported circuits. Hereby implementing the various comparator circuits, from the experimental results it is observed there was a 32 % reduction in power and the comparator design was 29 % faster as compared to the conventional circuit. Also, we can optimize the results by carefully improving the gain of the preamplifier stage for further better performance as compared to the reference comparators as given in Table II. From this table, we found out that the 28T comparator circuit improves the speed of the comparator by nearly 50 %. From the table, 19T comparator was found to be the most power-efficient also gives greater speeds. Also, all the comparators have been able to optimize differential signals as low as 2.7 mV.

## 4 Conclusions

In this work, various comparator circuits are studied and optimized in terms of power dissipation and delay and implemented using the cadence virtuoso tool. In the presented work most of the comparators are having lesser power consumption and higher speed at the expense of extra area on the chip which is one of the major constraints while we are trying to occupy more transistors in a smaller area. This can be achieved by making changes in the clock control circuitry. The implemented approach is better in form of increased comparison speed and power efficiency. The results show that offset voltage which is one of the most important criteria for precise application of comparator is changing with power and delay of the comparator and can make the circuit more power-hungry if the offset voltage and power are not optimized. Sizing the input transistors is of utmost importance and should be optimized for achieving low offset voltage as well as lower speed and power consumption. The preamplifier gain is one of the important factors which not only helps in making the circuit work efficiently at lower offset voltage but also improves the performance of the comparator by the reduction in comparison time. From the experimental results, it is observed that the 28T comparator circuit improves the speed by nearly

50%. At the same time, the 19T comparator was found to be the most power-efficient and also gives greater speeds. By further optimizing the circuit for a better preamplifier, a better comparator structure can be designed. Also, the combination of different latches and preamplifiers can give rise to better design alternatives. The clock control circuit can also be modified so that using a lesser number of transistors meaning the improved area can also be achieved with comparable performance. In the future using these above techniques, we can optimize further and it will suitable for even lower offset voltages.

## References


1 Sonar S, Vaithiyanathan D & Mishra A, *J Phys Conf Ser*, 1706 (2020) 1.

2 Varshney V & Nagaria R K, *AEU - Int J Electron Commun*, 116 (2020) 153068.

3 D'Amico S, Cocciolo G, Spagnolo A, De Matteis M & Baschirotto A, *IEEE Trans Instrum Meas*, 63 (2014) 295.

4 Gandhi P P & Devashrayee N M, *Anal Integr Circuits Signal Process*, 96 (2018) 147.

5 Khorami A & Sharifkhani M, *AEU - Int J Electron Commun*, 69 (2015) 1599.

6 Lu J & Holleman J, *IEEE Trans Circuits Syst I: Reg Papers*, 60 (2013) 1158.

7 Khorami A & Sharifkhani M, *Microelectron J*, 64 (2017) 45.

8 Khorami A & Sharifkhani M, Electron Lett, 52 (2016) 509.

9 Khorami A, Dastjerdi M B &. Ahmadi A F, *IEEE Int Symp Circuits Syst*, (2016) 2010.

10 Khorami A & Sharifkhani M, *IEEE Trans Very Large Scale Integr Syst*, 26 (2018) 2038.

11 Dubey A K & Nagaria R K, *J Circuits Syst Comput*, 27 (2018) 1850204.

12 Dubey A K & Nagaria R K, *Anal Integr Circuits Signal Process*, 101 (2019) 307.

13 Gao J, Li G & Li Q, *Electron Lett*, 51 (2015) 134.

14 Miyahara M & Matsuzawa A, *IEEE Asian Solid-State Circuits Conf*, (2009) 233.

15 Babayan-Mashhadi S & Lotfi R, *IEEE Trans Very Large Scale Integr Syst*, 22 (2014) 343.

16 Naseri H & Timarchi S, *IEEE Trans Very Large Scale Integr Syst*, 26 (2018) 1481.

17 Zhuang H, Cao W, Peng X & Tang H, *IEEE Trans Very Large Scale Integr Syst*, 29 (2021) 1485.

18 Wang Y, Yao M, Guo B, Wu Z, Fan W & Liou J J, *IEEE Access*, 7 (2019) 93396.