Indian Journal of Pure & Applied Physics
Vol. 53, July 2015, pp. 470-477

Current-mode MISO filter using CCCDTAs and grounded capacitors

Amornchai Chaichana[1]*, Adirek Jantakun[3], Montree Kumngern[1] & Winai Jaikla[2]

[1]Department of Telecommunications Engineering, Faculty of Engineering,
[2]Department of Engineering Education, Faculty of Industrial Education,
King Mongkut's Institute of Technology Ladkrabang, Bangkok 10520, Thailand,

[3]Department of Electronics and Telecommunication Engineering, Faculty of Engineering,
Rajamangala University of Technology Isan, Khonkaen Campus, Khonkaen, 40000, Thailand

*E-mail: kcamornc@kmitl.ac.th, kkmontre@kmitl.ac.th, mr.adirek@hotmail.com, kawinai@kmitl.ac.th

Received 12 May 2014; revised 29 September 2014; accepted 22 January 2015

This paper presents the current-mode multi-input single-output (MISO) biquadratic filter using current-controlled current differencing tranconductance amplifier (CCCDTA) as an active building block. The proposed circuit comprises three CCCDTAs and two grounded capacitors performing completely standard functions: low-pass, high-pass, band-pass, band-reject and all-pass functions and does not require double input current signals as well as inverting input currents. The pole frequency and quality factor of the proposed circuit can be adjusted electronically/independently via *dc* bias currents. In addition, the filter circuit has low-input and high-output impedance which facilitates easy connecting for current-mode circuit. The proposed circuit uses all grounded capacitors which is very suitable to further develop into an integrated circuit and without requiring any matching condition. Moreover, the active and passive sensitivities are low. The PSPICE simulation results are included to show the workability of the proposed circuit.

Keywords: Current-mode, MISO filter, CCCDTA, Grounded capacitor

1 Introduction

An analog filters are extremely useful circuits in many applications such as in communication system, signal processing, instrument and measurement system[1-6] etc. Now a days, current-mode active building block is useful more than voltage-mode devices wherewith it has high performance such as wide bandwidth, higher slew-rate, greater linearity, wider dynamic range, simple circuitry[1-8] etc. Especially, it can be used at low voltage and low power which is suitable for integrated circuit (IC) implementation for applications in mobile or wireless communication systems[7-9]. From the advantages mentioned above, the active filter networks are mainly referred as current-mode circuits. Principally, the modern current-mode circuits must have the following features (i) low-input and high-output impedances that are easier to use cascading or directing load[3,5,13,19,21,22,24], (ii) avoid the use of an external resistor due to the loss of power consumption and chip area[10,14,22-25], (iii) use grounded capacitor to compensate the latent capacity at the node of circuit or output terminals and to reduce the chip area of IC[10,14,22-26,28,29]. The active filters which provide five standard filter responses including high-pass filter (HPF), low-pass filter (LPF), band-pass filter (BPF), band-rejected filter (BRF) or eliminate frequency and all-pass filter or phase-shifted signal (APF) in the same circuit topology are the main research topic now a days. Especially, various multi-input single-output (MISO) filter configurations have been paid attention in literature[10-32]. The review of previous MISO filter topology is in the following text. The circuits in[11-12,15,17,19,21,27,30] have high-output impedance that make them suitable for cascading or driving to load without additional current buffers. However, they use more than two external resistors which are not ideal for IC implementation[7]. Moreover, they are absent of electronic controllability for tuning the pole frequency (ω_0) and quality factor (Q). Although it can be used as digital potentiometer for instead of an external resistors but the circuits become complicated[8]. Some circuits in[10,20,23] are benefited to electronic tuning of ω_0 and Q by the parasitic resistance R_x or the transconductance gain g_m but they afflict from the requirement of double input current signals. In Refs.18, 25-26, 28-29 the ω_0 and Q can be electronically adjusted. Also they are not needed the external resistors as well as matching conditions which make them easier for tuning and fabricating in IC. However, the input nodes do not exhibit low impedance which is not ideal for current-mode configuration. The current-mode MISO filter in[31] can be electronically/independently controlled for ω_0 and Q. But, it uses an excessive number of active elements (five MCFTAs). The current-mode MISO filter presented in Ref. 32 has low-input and high-output impedance and can be electronically adjusted for ω_0 and Q. Unfortunately, the ω_0 and Q are inconvenient for independently or orthogonally tuning. The proposed current-mode MISO filters are compared with previously published[10-32] current-mode MISO filters and the results are presented in Table 1.

The current-mode MISO filter is presented and the proposed circuit provides the following advantageous features:

1 The output response of proposed circuit performs low-pass, high-pass, band-pass, band-reject and all-pass functions from the same circuit configuration without the requirement of double input current signals.
2 The proposed circuit has low-input and high-output impedance which is easy to cascade in high-order filter or drive load without using a buffering device.
3 The pole frequency and quality factor can be electronically/independently adjusted via *dc* bias current of CCCDTAs.
4 The proposed circuit uses only grounded capacitors, which is advantageous from the point of view of integrated circuit implementation and compensation of the latent capacity.
5 The active and passive sensitivities are low.

To verify the workability of the proposed current-mode MISO filter, the PSPICE simulation results of a BJT technology implementation have been included.

2 Principle of Proposed Circuit

2.1 Descriptions of CCCDTA

This section is a description of CCCDTA[33]. It was proposed by Siripruchyanun and Jaikla[34] which is similar to the conventional CDTA, except that CCCDTA has finite input resistances (R_p and R_n) at the p and n input terminal. The characteristic of voltages and currents of CCCDTA are shown in Eq. (1):

Table 1 — Comparison between various MISO filter

Ref	Active element	Number of active element	Number of R+C	Electronic control	Independent Tuned of ω_0 and Q	Requiring double input	Matching Condition	Low-input impedances	High-output impedance
[10]	CCCII	2	0+2	Yes	Yes	Yes	No	No	Yes
[11]	CCII	1	2+2	No	No	No	Yes	No	Yes
[12]	CFOA	1	4+2	No	No	No	Yes	No	Yes
[13]	CDTA	4	2+2	Yes	No	No	No	Yes	Yes
[14]	CCDDCC	3	0+2	Yes	Yes	No	No	No	Yes
[15]	MO-CCII + MO-CCCA	3	2+2	Yes	Yes	No	No	No	Yes
[16]	DVCCTA	1	1+2	Yes	No	No	No	No	Yes
[17]	CCII	3	3+2	No	Yes	No	No	No	Yes
[18]	OTA	5	0+2	Yes	No	No	No	No	Yes
[19]	CDBA	3	2+2	No	No	No	No	Yes	Yes
[20]	DO-CCCII	2	0+2	Yes	No	Yes	No	No	Yes
[21]	CDBA	3	2+2	No	No	Yes	No	Yes	Yes
[22]	CDTA	3	0+2	Yes	No	No	No	Yes	Yes
[23]	CCCDTA	1	0+2	Yes	No	Yes	No	No	Yes
[24]	CDTA	4	2+2	Yes	Yes	No	No	Yes	Yes
[25]	MO-CCCCTA	2	0+2	Yes	No	No	No	No	Yes
[26]	CCCII	2	0+2	Yes	No	No	No	No	Yes
[27]	DO-ICCII	3	3+2	No	No	No	No	No	Yes
[28]	CCCCTA	2	0+2	Yes	Yes	No	No	No	Yes
[29]	CCCCTA	2	0+2	Yes	Yes	No	No	No	Yes
[30]	FDCCII	1	2+2	No	No	No	No	No	Yes
[31]	MCFTA	5	0+2	Yes	Yes	No	No	Yes	Yes
[32]	ZC-CDTA	3	0+2	Yes	No	No	No	Yes	Yes
Proposed MISO	CCCDTA	3	0+2	Yes	Yes	No	No	Yes	Yes

$$\begin{bmatrix} V_p \\ V_n \\ I_z \\ I_x \end{bmatrix} = \begin{bmatrix} R_p & 0 & 0 & 0 \\ 0 & R_n & 0 & 0 \\ 1 & -1 & 0 & 0 \\ 0 & 0 & 0 & \pm g_m \end{bmatrix} \begin{bmatrix} I_p \\ I_n \\ V_x \\ V_z \end{bmatrix} \qquad \ldots(1)$$

For the CCCDTA implemented by a BJT technology, the parasitic resistances (R_p and R_n) and transconductance g_m can be expressed to be:

$$R_p = R_n = \frac{V_T}{2I_{B1}} \qquad \ldots(2)$$

and

$$g_m = \frac{I_{B2}}{2V_T} \qquad \ldots(3)$$

V_T is the thermal voltage. From Eqs (2) and (3), it can be seen that the parasitic resistances can be tuned by adjusting the *dc* bias current I_{B1} and the transconductance can be tuned by adjusting the *dc* bias current I_{B2}. The symbol and the equivalent circuit of the CCCDTA are shown in Figs 1(a) and (b), respectively.

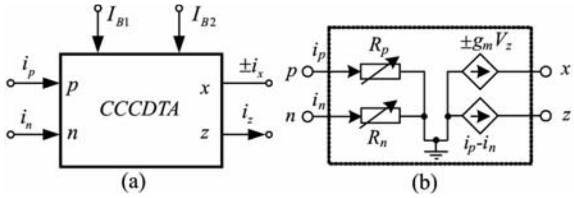

Fig. 1 — CCCDTA (a) Symbol (b) Equivalent circuit

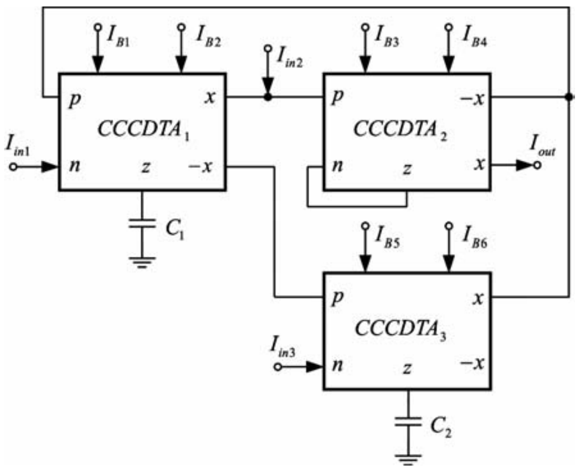

Fig. 2 — Proposed MISO filter

2.2 Proposed Current-mode MISO Filter

The proposed current-mode MISO filter is shown in Fig. 2. It consists of 3 CCCDTAs and 2 grounded capacitors, which is advantageous from the point of view of integrated circuit implementation since grounded capacitors can be reduced the area for ICs implementation and compensated the stay of capacitance at node or output terminals of CCCDTAs. From the CCCDTA properties, the output current can be given as:

$$I_{out} = k\left(\frac{-I_{in1}\dfrac{C_2}{g_{m3}}s + I_{in2}\left[\dfrac{C_1C_2}{g_{m1}g_{m3}}s^2+1\right] - I_{in3}}{\dfrac{C_1C_2}{g_{m1}g_{m3}}s^2 + \dfrac{C_2k}{g_{m3}}s+1}\right) \qquad \ldots(4)$$

where $k = \frac{g_{m2}R_{n2}}{2}$. According to Eq. (4), the selection of three input currents I_{in1}, I_{in2} and I_{in3} to obtain five standard second order filters, inverting LPF, HPF, inverting BPF, BRF and APF functions are achieved in Table 2. It is clear that the output-current filter responses obtain a standard biquadratic function without requirement of double input current signals as well as inverting input currents, that is easy to choose the output filter response without requirement of modifying circuit and additional double or inverting amplifier. Moreover, the selection can be digitally controlled by using the digital selection circuit in Ref. 35.

Table 2 — Input selection to obtain output filter response of proposed circuit

Filter Response I_{out}	Input Selection I_{in1}	I_{in2}	I_{in3}
LPF	0	0	1
HPF	0	1	1
BPF	1	0	0
BRF	0	1	0
APF	1	1	0

Furthermore, the pole frequency (ω_0) and quality factor (Q) are written as:

$$\omega_0 = \sqrt{\frac{g_{m1}g_{m3}}{C_1C_2}} \qquad \ldots(5)$$

and

$$Q = \frac{2}{g_{m2}R_{n2}}\sqrt{\frac{C_1 g_{m3}}{C_2 g_{m1}}} \qquad \ldots(6)$$

Substituting the parasitic resistance $R_{n2} = (V_T / 2I_{B3})$ and transconductance $g_{m1} = (I_{B2} / 2V_T)$, $g_{m2} = (I_{B4} / 2V_T)$ and $g_{m3} = (I_{B6} / 2V_T)$ into Eqs (5) and (6), the ω_0 and Q can be expressed as:

$$\omega_0 = \frac{1}{2V_T}\sqrt{\frac{I_{B2}I_{B6}}{C_1C_2}} \quad \ldots(7)$$

and

$$Q = \frac{8I_{B3}}{I_{B4}}\sqrt{\frac{C_1I_{B6}}{C_2I_{B2}}} \quad \ldots(8)$$

It is evident from Eqs (7) and (8) that the ω_0 and Q can be electronically controlled by adjusting the *dc* bias currents of CCCDTAs. Moreover, if $I_{B2} = I_{B6} = I_B$ (in practically, this can be achieved by using current mirror to copy current I_B to I_{B2} and I_{B6}), the ω_0 can be adjusted independently and linearly without effecting of the Q values. Also, the Q can be adjusted independently by changing I_{B3} and I_{B4} without disturbing ω_0. Then, Q is higher by varying I_{B3} more than I_{B4} as described in Eqs (8) and (9).

$$\omega_0 = \frac{I_B}{2V_T}\sqrt{\frac{1}{C_1C_2}} \quad \ldots(9)$$

and

$$Q = \frac{8I_{B3}}{I_{B4}}\sqrt{\frac{C_1}{C_2}} \quad \ldots(10)$$

Additionally, the current input nodes I_{in1} and I_{in3} exhibit low impedance by setting I_{B1} and I_{B5} as high as possible. Furthermore, the output current node I_{out} has high-impedance which is easy to directly connecting to load or cascading to high order of filters without using the current buffer devices that make it ideal for using in current-mode configuration. As a drawback, the impedance of input current node I_{in2} is not of low impedance character. It depends on the adjusting of R_{p2} and R_{n2} (ideally, they are equal). Thus, if the tuning of Q is done by adjusting I_{B3}, the impedance at current input node I_{in2} is also changed. To alleviate this effect, the tuning of Q should be done by adjusting I_{B4}.

2.3 Sensitivities of Proposed MISO Filter

The sensitivities of the active and passive elements of MISO filter are low as given in Eqs(11 and 12):

$$S_{V_T}^{\omega_0} = -1,\ S_{I_{B2},I_{B6}}^{\omega_0} = \frac{1}{2},\ S_{C_1,C_2}^{\omega_0} = -\frac{1}{2} \quad \ldots(11)$$

and

$$S_{I_{B3}}^{Q} = 1,\ S_{I_{B4}}^{Q} = -1,\ S_{C_1,I_{B6}}^{Q} = \frac{1}{2},\ S_{C_2,I_{B2}}^{Q} = -\frac{1}{2} \quad \ldots(12)$$

It is to be noted that the relative sensitivities of the proposed circuit are equal or less than unity in magnitude.

2.4 Non-ideal Effects

It is necessary to take into account the non-ideal effects of CCCDTA on proposed MISO filter, which are voltage/current tracking errors and parasitic elements. The first effect comes from tracking errors of current differencing amplifiers and transconductance amplifiers[23,33]. These tracking errors are caused by the mismatch of transistors in internal construction of CCCDTA. The characteristic of voltages and currents of CCCDTA are modified as:

$$\begin{bmatrix} V_p \\ V_n \\ I_z \\ I_x \end{bmatrix} = \begin{bmatrix} R_p & 0 & 0 & 0 \\ 0 & R_n & 0 & 0 \\ \alpha_p & -\alpha_n & 0 & 0 \\ 0 & 0 & 0 & \pm\beta g_m \end{bmatrix} \begin{bmatrix} I_p \\ I_n \\ V_x \\ V_z \end{bmatrix} \quad \ldots(13)$$

where α_p and α_n are tracking error of the current transfer gains from p, n terminals to z terminal, respectively. β is the tracking error of the transconductance gains. The output current of the proposed circuit is shown in Fig. 2, get modified to:

$$I_{out} = \frac{\beta_2\alpha_{p2}g_{m2}R_{n2}}{2}\left(\frac{-I_{in1}\dfrac{\alpha_{n1}C_2}{\beta_3\alpha_{p1}\alpha_{p2}g_{m3}}s + I_{in2}\left(\dfrac{C_1C_2}{\beta_1\beta_3\alpha_{p1}\alpha_{p2}g_{m1}g_{m3}}s^2 + 1\right) - I_{in3}\dfrac{\alpha_{n3}}{\alpha_{p2}}}{\dfrac{C_1C_2}{\beta_1\beta_3\alpha_{p1}\alpha_{p2}g_{m1}g_{m3}}s^2 + \dfrac{\beta_2 g_{m2}C_2R_{n2}}{2\beta_3 g_{m3}}s + 1} \right) \quad \ldots(14)$$

Then, the ω_0 and Q of the proposed circuit become:

$$\omega_0 = \frac{1}{2V_T}\sqrt{\frac{\beta_1\beta_3\alpha_{p1}\alpha_{p2}I_{B2}I_{B6}}{C_1C_2}}, \qquad \ldots(15)$$

and

$$Q = \frac{8I_{B3}}{\beta_2 I_{B4}}\sqrt{\frac{\beta_3 C_1 I_{B6}}{\beta_1\alpha_{p1}\alpha_{p2}C_2 I_{B2}}}. \qquad \ldots(16)$$

The second effect comes from parasitic elements of CCCDTA. The parasitic resistances and capacitances at high-impedance terminals affect the ω_0 and Q of the proposed circuit. There are R_z, C_z at z terminal and R_x, C_x at x terminal. The proposed circuit with parasitic elements is shown in Fig. 3. Then, the output current is obtained as:

$$I_{out} = k\left\{\frac{-\frac{Y_2}{g_{m3}}\left(1+Y_6R_{p1}\right)\left(1+Y_3R_{p3}\right)I_{in1} + \left[\frac{Y_1Y_2}{g_{m1}g_{m3}}\left(1+Y_6R_{p1}\right)\left(1+Y_3R_{p3}\right)+1\right]I_{in2} - \left(1+Y_3R_{p3}\right)I_{in3}}{\frac{Y_1Y_2}{g_{m1}g_{m3}}\left(1+Y_6R_{p1}\right)\left(1+Y_3R_{p3}\right) + k\frac{Y_2}{g_{m3}}\left(1+Y_3R_{p3}\right)+1}\right\} \qquad \ldots(17)$$

where

$k = \frac{g_{m2}R_{n2}}{\left(2+R_{n2}Y_5\right)\left(1+Y_4R_{p2}\right)}$, $Y_1 = s\left(C_1+C_{z1}\right)+G_{z1}$,

$Y_2 = s\left(C_2+C_{z3}\right)+G_{z3}$, $Y_3 = Y_4 = sC_{x1}+G_{x1}$,

$Y_5 = sC_{z2}+G_{z2}$ and $Y_6 = s\left(C_{x2}+C_{x3}\right)+G_{x2}+G_{x3}$.

From Eq. (16), if the operational frequency (f_o) is more lower than $\frac{G_{x1}R_{p2}+1}{2\pi C_{x1}R_{p2}}$, $\frac{G_{x1}R_{p3}+1}{2\pi C_{x1}R_{p3}}$, $\frac{G_{z2}R_{n2}+1}{2\pi C_{z2}R_{n2}}$, $\frac{\left(G_{x2}+G_{x3}\right)R_{p1}+1}{2\pi\left(C_{x2}+C_{x3}\right)R_{p1}}$ and $R_{p1}\cong 0$, $R_{p3}\cong 0$ (in practically, this can be achieved by setting I_{B1} and I_{B5} as high as possible or carefully designing the internal construction of CCCDTA to:

$$I_{out} = k\left(\frac{-I_{in1}\frac{\left(sC_2^*+G_{z3}\right)}{g_{m3}} + I_{in2}\left(\frac{s^2C_1^*C_2^* + s\left(C_1^*G_{z3}+C_2^*G_{z1}\right) + G_{z1}G_{z3}+g_{m1}g_{m3}}{g_{m1}g_{m3}}\right) - I_{in3}}{s^2\frac{C_1^*C_2^*}{g_{m1}g_{m3}} + s\frac{kg_{m1}C_2^*+C_1^*G_{z3}+C_2^*G_{z1}}{g_{m1}g_{m3}} + \frac{G_{z1}G_{z3}+kg_{m1}G_{z3}+g_{m1}g_{m3}}{g_{m1}g_{m3}}}\right) \qquad \ldots(18)$$

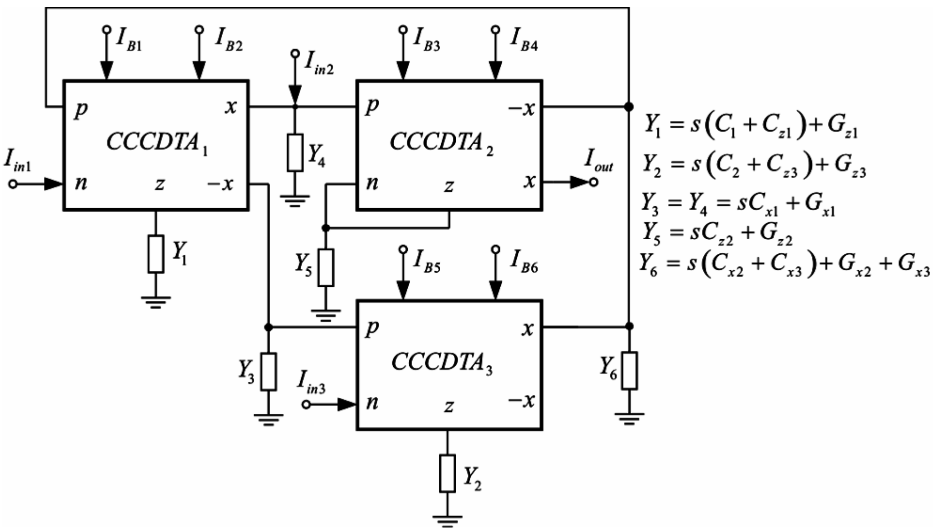

Fig. 3 — Model of circuit for high frequency analysis

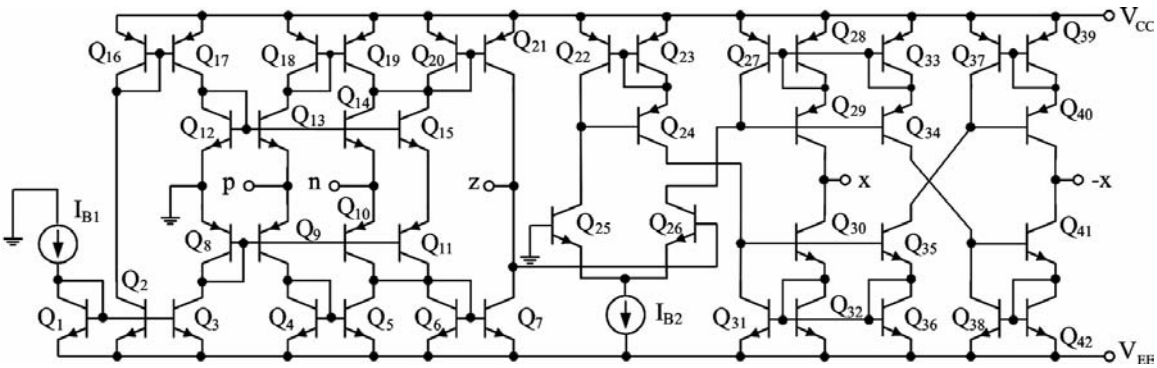

Fig. 4 — Internal construction of CCCDTA

where $k = \frac{g_{m2}R_{n2}}{2}$, $C_1^* = C_1 + C_{z1}$ and $C_2^* = C_2 + C_{z3}$.

The ω_0 and Q of the proposed circuit changed to:

$$\omega_0 = \sqrt{\frac{G_{z1}G_{z3} + kg_{m1}G_{z3} + g_{m1}g_{m3}}{C_1^* C_1^*}} \quad \ldots(19)$$

and

$$Q = \frac{g_{m1}g_{m3}}{kg_{m1}C_2^* + C_1^* G_{z3} + C_2^* G_{z1}} \times \sqrt{\frac{G_{z1}G_{z3} + kg_{m1}G_{z3} + g_{m1}g_{m3}}{C_1^* C_2^*}} \quad \ldots(20)$$

3 PSPICE Simulations Results

To verify the theoretical analysis of the proposed circuit as shown in Fig. 2, it was simulated using the *pnp* and *npn* transistors by the PR200N and NR200N bipolar transistors of ALA400 transistor array from AT&T. Internal construction of CCCDTA used in simulation as shown in Fig. 4. The power supply voltage was taken as ±1.5 V and the capacitors of the configuration values were chosen as $C_1 = C_2 = 0.3$nF. The simulation set for $Q = 1$ and $f_0 = 510.111$ kHz with I_{B1} = 100 µA, I_{B3} = 25 µA, I_{B4} = 200 µA, I_{B5} = 100 µA and $I_{B2} = I_{B6} = I_B = 50$ µA. Figure 5(a) shows the frequency response of output-current gain of the BPF, LPF, HPF and BRF, dependent on selection as presented in Table 2, without modifying circuit topology. Furthermore, the simulation results of gain and phase response of APF are shown in Fig. 5 (b). The simulated pole frequency of the proposed circuit was obtained as 483.509 kHz, while the calculated value from Eq. (7) is about 510.111 kHz (deviated about 5.21%). The deviation has been affected from error of voltage, current transfer gains and the parasitic elements of the CCCDTAs. The results in Fig. 6 show the tuning of Q for the BPF response by electronics adjusting at Q = 1, 2.5, 4, 8 and 16, when kept to be I_{B4} = 200 µA and varied I_{B3}, as 25, 50, 100, 200 and 400 µA, respectively. Figure 7 shows the Q of the BPF response for difference values of I_{B4} as 25, 50, 100, 200 and 400 µA, respectively, while I_{B3} = 25 µA. The results of the Q are varied from 8, 4, 2, 1 and 0.5, respectively. These results are confirmed that Q can be electronically adjusted without affecting of pole frequency, as shown in Figs (7) and (8). Figure 8 shows the pole frequency of the BPF response varied as 118.577, 238.781, 483.059 and 990.832 kHz for

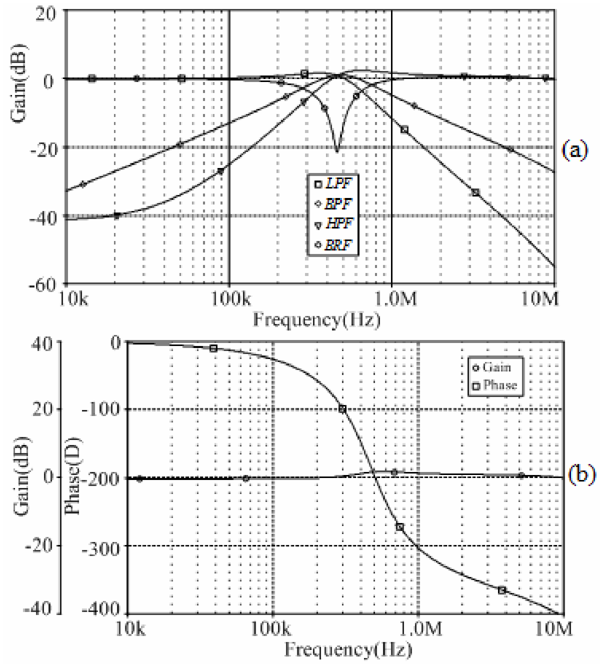

Fig. 5 — Frequency response of current-mode MISO filter (a) BPF, LPF, HPF and BRF (b) APF

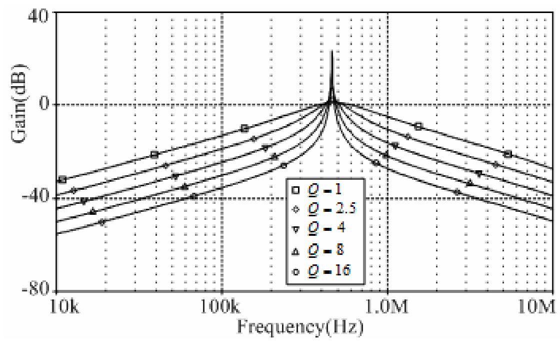

Fig. 6 — Varied value of Q for BPF responses at different values of I_{B3}

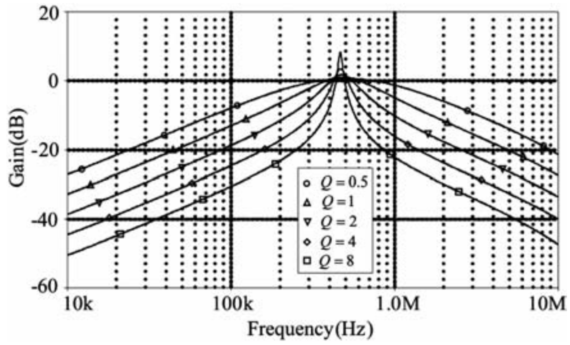

Fig. 7 — Varied value of Q for BPF responses at different values of I_{B4}

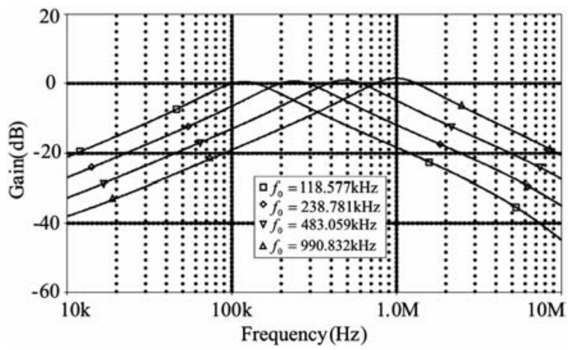

Fig. 8 — BPF responses at different values of I_B

value of I_B as 12.5, 25, 50 and 100 μA, respectively. It can be seen that the pole frequency can be electronically adjusted without influence of the quality factor by *dc* bias current I_B.

The tolerance of capacitors may result in the pole frequency deviation from the requirement. In this case, a Monte Carlo analysis can be used for analyzing the error from the tolerance. The statistical results of a Monte Carlo analysis within 5% tolerances to all the capacitors by using the Gaussian probability distribution and 200 trials are shown in

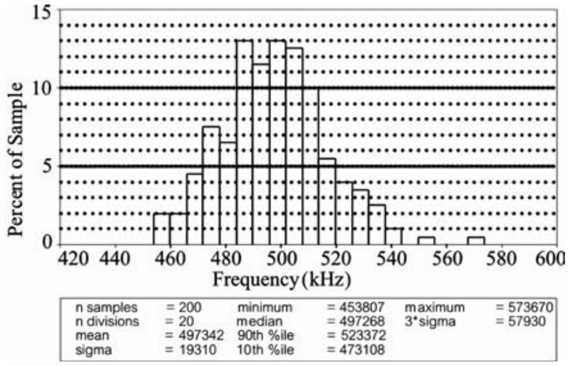

Fig. 9 — Histograms of the possible spread of the pole frequency

Fig. 9. The histograms of the possible spread of the pole frequency are shown in Fig. 9. The standard deviation of the pole frequency of BPF response is 19.310 kHz. The possibility for the maximum and minimum of the pole frequency are 573.679 kHz and 453.807 kHz, respectively.

4 Conclusions

A current-mode MISO filter using CCCDTAs and grounded capacitors has been presented. The proposed current-mode MISO filter consists of three CCCDTAs and two grounded capacitors and offers the following advantages: (i) it performs low-pass, high-pass, band-pass, band-rejected and all-pass functions from the same configuration, without requirement of double input current signals and inverting input currents (ii) the pole frequency and quality factor can be independently adjusted with bias currents, (ii) the employment of two grounded capacitors, which is attractive for either IC implementation (iv) the active and passive sensitivities are low (v) availability of explicit low-input and high-output impedances, enables easy cascading in high-order filter or driving load without external current buffers (vi) the quality factor is high possibility by adjusting the *dc* bias currents. The PSPICE simulation results agree well with the theoretical anticipation.

References

1 Toumazou C, Lidgey F J & Haigh D G, *Peter Peregrinus*, (1990).
2 Biolek D, Biolkova V & Kolka Z, *Indian J Pure & Appl Phys*, 47 (2009) 535.
3 Horng J W, Hou C L, Guo Y S, Hsu C H, Yang D Y & Ho M J, *Circuits and Systems,* 3, (2012) 176.
4 Horng J W, Wu C M & Herencsar N, *Indian J Pure & Appl Phys*, 52 (2014) 556.
5 Jerabek J & Vrba K, *International Journal of Electronics and Communication (AEU*), 64 (2010) 588.

6 Maheshwari S, *Wseas Transections on Electronics*, 5 (2008) 238.
7 Tangsrirat W, Mongkolwai P & Pukkalanun T, *Indian J Pure & Appl Phys*, 50 (2012) 600.
8 Sotner R, Herencsar N, Jerabek J, Dvorak R, Kartci A, Dostal T & Vrba K, *J of electrical engineering*, 64 (2013) 65.
9 Sotner R, Lahiri A, Kartci A, Herencsar N, Jerabek J & Vrba K, *Advances in Electrical and Computer Engineering*, 13 (2013) 65.
10 Kumngern M, *Journal of Electrical and Electronics Engineering Research*, 3 (2011) 162.
11 Özcan S, Kuntman H & Çicekoglu O, *Computers and Electrical Engineering,* 29 (2003) 45.
12 Sharma R K & Senani R, "*International Journal of Electronics and Communication (AEU),* 57 (2003) 301.
13 Uygur A, Kuntman H & Zeki A, *The 4th International Conference on Electrical and Electronics*, (2005) 46.
14 Prommee P, Somdunyakanok M & Toomsawasdi S, *2010 IEEE International Symposium on Components, Circuits, Devices & Systems*, (2011) 1045.
15 Chunhua W, Haiguang L & Yan Z, *International Journal of Electronics and Commun (AEU)* 63, (2009) 448.
16 Pandey N & Paul S K, *Active and Passive Electronic Components*, (2011) Article ID 929507.
17 Horng J W, *Microelectronics Journal*, 42 (2011) 693.
18 LEE C N, *Circuits, Systems & Signal Processing*, 29 (2010) 263.
19 Tangsrirat W & Surakampontorn W, *Frequenz,* 50 (2006) 152.
20 Siripruchyanun M & Jaikla W, *Active and Passive Electronic Components* (2007) Article ID 36849.
21 Sawangarom V, Dumawipata T, Tangsrirat W & Surakampontorn W, *The 2007 ECTI International Conference, Thailand*, (2007) 53.
22 Tangsrirat W, *J of Active and Passive Electronic Devices,* 4 (2009) 135.
23 Siripruchyanun M & Jaikla W, *Circuits, Systems & Signal Processing*, 27 (2008) 113.
24 Tangsrirat W & Pukkalanun T, *International J of Circuit Theory and Appl*, 39 (2011) 31.
25 Singh S V, Maheshwari S & Chauhan D S, *Int. J. on Electrical and Power Engineering*, 1 (2010) 36.
26 Tangsrirat W & Channumsin O, *Indian J Pure & Appl Phys*, 49 (2011) 137.
27 Chen H P, *Indian J Pure & Appl Phys*, 50 (2012) 188.
28 Singh S V & Maheshwari S, *Radioengineering,* 21 (2012) 317.
29 Jaikla W, Siripongdee S & Suwanjan P, *Radioengineering*, 21 (2012) 886.
30 Kacar F, Yesil A and Kuntman H, *Radioengineering*, 21 (2012) 1269.
31 Nei X & Pan Z, *Microelectronics Journal,* 44 (2013) 802.
32 Kumngern M & Dejhan K, *2012 Second International Conference on Digital Information and Communication Technology and it's Applications (DICTAP),* (2012) 309.
33 Siripruchyanun M & Jaikla W, *ECTI Transactions on Electrical Engineering, Electronics, and Communications,* 5 (2007) 41.
34 Biolek D, *The European conference on circuit theory and design*, (2003) 397.
35 Tangsrirat W, *International Journal of Electronics and Communication*, 62 (2008) 97.