Indian Journal of Pure & Applied Physics
Vol. 53, May 2015, pp. 341-349

Design and experiment of VDCC-based voltage mode universal filter

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Received 22 May 2014; revised 24 November 2014; accepted 2 March 2015

In the present paper, configurations of the three new voltage-mode universal biquad filters are presented. The first filter is three-inputs single-output (TISO) filter which can realize all the five standard types of biquadratic functions in voltage-mode that is low-pass, band-pass, high-pass, band-stop and all-pass filter with single VDCC. The second filter has single-input and dual-output, which can also simultaneously realize the high-pass and band-pass filter functions. The third circuit is universal filter with single-input and dual-output, which can simultaneously realize low-pass and band-pass filters. Simulation results are given to confirm the theoretical analysis. The presented biquad filters are simulated using TSMC CMOS 0.18 μm technology. To realize TISO filter with discrete elements VDCC block experimentally generated with operational transconductance amplifier, OPA860. Experimental results of the filter agreed well with the theoretical analysis and SPICE simulations.

Keywords: VDCC, Voltage-mode filter, Biquad filter, Parasitic and non-ideal analyses, Operational transconductance amplifier

1 Introduction

Multi-function type active filters are especially versatile, since the same topology can be used for different filter functions. Several voltage-mode biquad filter[1-21] circuits using different active elements such as current conveyors[1] (CCIs), universal voltage conveyors[2] (UVCs), second generation current conveyors[3] (CCIIs), inverting second generation current conveyors[4] (ICCIIs),current feedback operational amplifiers[5,6] (CFOAs), four terminal floating nullors[7] (FTFNs), differential voltage current conveyors[8-10] (DVCCs), differential difference current conveyors [11] (DDCCs), current differencing buffered amplifiers[12,13] (CDBAs), operational transconductance amplifier[14-17] (OTAs), fully differential current conveyor[18-20] (FDCCII) and voltage differencing buffered amplifier[21] (VDBA) have been reported in the literature. In contrast with voltage-mode biquad filters (TISO and SIDO), they suffer from one or more of the following drawbacks:

(i) They need a large number of active components[2,4,5,8,10,11,13-17,20,21]; (ii) They include four or more passive elements[1-12,18-20]; (iii) Some of filter response requires the component-matching conditions[1,3,9,12]; (iv) Pole frequency cannot be tuned electronically[1-7,9-12,18,19]; (v) Quality factor cannot be adjusted as independent frequency[1,3,4,9,11,13,15,16,18,20,21].

Recently, various active building blocks have been introduced in Ref. 22, where the voltage differencing current conveyor (VDCC) is useful. A CMOS implementation of VDCC has been proposed and grounded inductance simulators based VDCC have been given as its application[23]. Also, second order multiphase oscillator[24] has been proposed based on modified VDCC. New VDCC-based biquad filter circuits with minimum number of grounded passive elements have been studied in the present paper.

Three voltage mode biquad filters which contain single VDCC and few passive elements have been presented. The first circuit is a universal filter with three-inputs single-output, which can realize voltage-mode low-pass, band-pass, high-pass, band-stop and all-pass filter responses employing single VDCC. The second universal filter has single-input and dual-output, which can also realize the high-pass and band-pass filter functions, simultaneously. The third universal filter circuit with single-input and dual-output, which can simultaneously realize low-pass and band-pass filters. Quality factor of the last two filters can be changed by adjusting one resistor without effecting pole frequency. Furthermore, each of the circuits still enjoys realization using a minimum number of active and passive components, and no passive element matching requirement to realize specific filtering functions. For all filters, pole

frequency can be tuned electronically with changing bias current. The performances of the VDCC and voltage-mode biquad filters are illustrated by SPICE simulations. To realize TISO filter with discrete elements VDCC block experimentally generated with a commercially available versatile monolithic component OPA860, which includes wideband, bipolar operational transconductance amplifier (OTA) and voltage buffer amplifier. Experimental results of the filter agreed well with the theoretical analysis and SPICE simulations.

2 Proposed Circuit

The circuit symbol of the recently proposed active element, VDCC, is shown in Fig. 1, where P and N are input terminals and Z, X, W_P and W_N are output terminals[23]. All of the terminals exhibit high impedance, except the X terminal.

$$\begin{bmatrix} I_P \\ I_N \\ I_Z \\ V_Z \\ I_{W_P} \\ I_{W_N} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ \alpha g_m & -\alpha g_m & 0 & 0 \\ 0 & 0 & \beta & 0 \\ 0 & 0 & 0 & \gamma_{W_P} \\ 0 & 0 & 0 & -\gamma_{W_N} \end{bmatrix} \begin{bmatrix} V_P \\ V_N \\ V_X \\ I_X \end{bmatrix} \quad \ldots(1)$$

where α, β and γ are non-ideal voltage and current gains of VDCC which ideally equal to one. g_m is transconductance gain of the VDCC defined by:

$$g_m = \sqrt{I_{B1}\mu_n C_{ox}\left(\frac{W}{L}\right)_1} \quad \ldots(2)$$

where μ_n is the mobility of the carrier for NMOS transistors, C_{ox} the gate-oxide capacitance per unit area, W the effective channel width, L the effective channel length and I_{B1} is bias current.

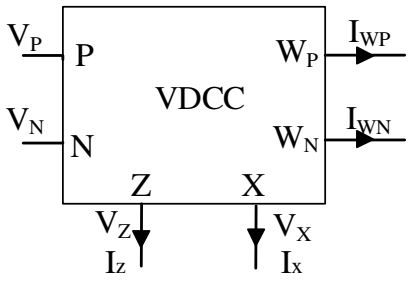

Fig. 1 — Circuit symbol of the VDCC

The filter topology in Fig. 2 is compact version, employed only with VDCC element in the filter[16]. The filter can be used as three-inputs single-output (TISO) voltage-mode filter as shown in Fig. 2. Circuit analysis yields the following for the output voltage which can be expressed as:

$$V_{OUT} = \frac{V_2 s^2 C_1 C_2 + V_1 s C_2 g_m + V_3 g_m G}{s^2 C_1 C_2 + s C_2 g_m + g_m G} \quad \ldots(3)$$

Depending on the voltage status of V_1, V_2 and V_3 in the numerator of Eq. (3), one of the following five filter functions is realized:

(i) LP: $V_1 = V_2 = 0$, $V_3 = V_{IN}$
(ii) BP: $V_2 = V_3 = 0$, $V_1 = V_{IN}$
(iii) HP: $V_1 = V_3 = 0$, $V_2 = V_{IN}$
(iv) BS: $V_1 = 0$, $V_2 = V_3 = V_{IN}$
(v) AP: $V_2 = V_3 = -V_1 = V_{IN}$

The circuit of quality factor (Q) and pole frequency (ω_0) can be given as follows:

$$Q = \sqrt{\frac{G C_1}{g_m C_2}} \quad \ldots(4)$$

$$\omega_0 = \sqrt{\frac{g_m G}{C_1 C_2}} \quad \ldots(5)$$

The other single-input dual-output (SIDO) two voltage-mode multifunction filters, employing a single voltage differencing current conveyor are shown in Fig. 3. Two of these configurations use two capacitors and two resistors.

The first SIDO voltage-mode multifunction filter is shown in Fig. 3(a). Circuit analysis yields the

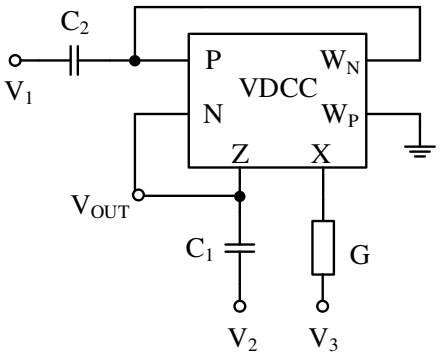

Fig. 2 — TISO biquad filter

following SIDO voltage-mode filter transfer functions:

$$HP \rightarrow \frac{V_{01}}{V_1} = \frac{s^2 C_1 C_2}{s^2 C_1 C_2 + s C_1 G_2 + g_m G_1} \quad \ldots(6)$$

$$BP \rightarrow \frac{V_{02}}{V_1} = \frac{s C_2 g_m}{s^2 C_1 C_2 + s C_1 G_2 + g_m G_1} \quad \ldots(7)$$

The second SIDO voltage-mode multifunction filter is shown in Fig. 3(b). Circuit analysis yields the following SIDO voltage-mode filter transfer functions:

$$BP \rightarrow \frac{V_{01}}{V_1} = \frac{s C_1 G_2}{s^2 C_1 C_2 + s C_1 G_2 + g_m G_1} \quad \ldots(8)$$

$$LP \rightarrow \frac{V_{02}}{V_1} = \frac{g_m G_2}{s^2 C_1 C_2 + s C_1 G_2 + g_m G_1} \quad \ldots(9)$$

For two presented filter topology quality factor (Q) and pole frequency (ω_0) can be given as follows:

$$Q = \frac{1}{G_2}\sqrt{\frac{g_m G_1 C_2}{C_1}} \quad \ldots(10)$$

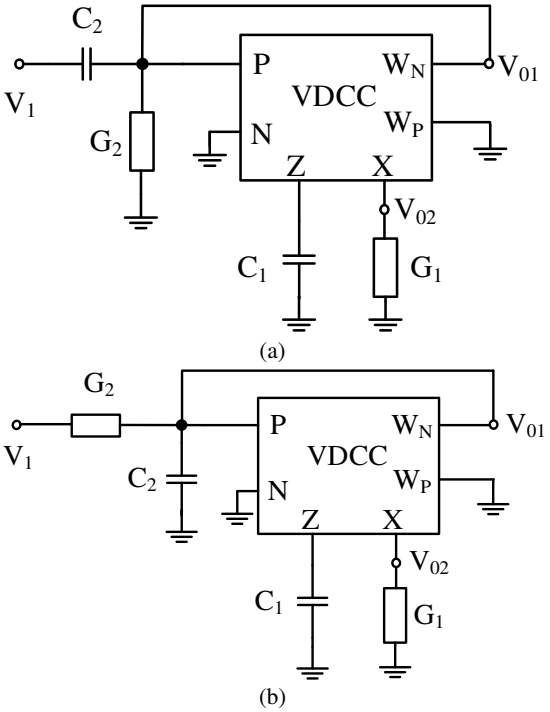

Fig. 3 — SIDO biquad filters

$$\omega_0 = \sqrt{\frac{g_m G_1}{C_1 C_2}} \quad \ldots(11)$$

Eq. (10) indicates that present filters are suitable for obtaining high-Q values. Firstly, high Q value is obtained when the value of G_2 is selected low. Moreover, G_2 can be employed NMOS transistors and adjusted electronically through the control voltages[25].

3 Effect of the Parasitic Impedances in VDCC

The effect of the parasitic impedance on the pole frequency and quality factor has been investigated to indicate performance of filters. For example, the three-inputs single-output voltage-mode filter as shown in Fig. 2 is taken into consideration where the modified topology together with parasitic impedances, is shown in Fig. 4.

In Fig. 4, the port W_N exhibits of high value parasitic resistance R_{P2}, in parallel with low value capacitance C_{P2}, the port X exhibit of low value parasitic serial resistance R_{P1} and the port Z exhibits of high value parasitic resistance R_{P3}. Taking into account the parasitic elements in Fig. 4, transfer function is obtained as:

$$V_{OUT} = V_2 \frac{s^2 C_1 C_{T2} + s C_1 G_{P2}}{\Delta s} + V_1 \frac{s C_2 g_m}{\Delta s} + V_3 \frac{g_m G_1}{\Delta s} \quad \ldots(12)$$

where $C_{T2}=C_2+C_{P2}$ and Δs is the characteristic equation given by:

$$\Delta s = s^2 C_1 C_{T2} + s\left(C_{T2}\left(g_m + G_{P3}\right) + C_1 G_{P2}\right) + g_m G_1 + G_{P2}\left(g_m + G_{P3}\right) \quad \ldots(13)$$

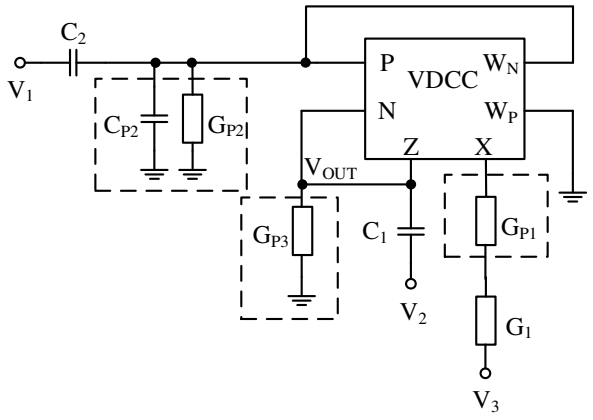

Fig. 4 — Parasitic impedance of VDCC affecting filter of Fig. 2

From the denominator of transfer function given in Eq. (13), the Q' and ω'_0 of the filter circuit of which parasitic effects are considered as given:

$$Q' = \frac{\sqrt{C_1 C_{T2}}\sqrt{g_m G_1 + G_{P2}\left(g_m + G_{P3}\right)}}{C_{T2}\left(g_m + G_{P3}\right) + C_1 G_{P2}} \quad \ldots(14)$$

$$\omega_0' = \sqrt{\frac{g_m G_1 + G_{P2}\left(g_m + G_{P3}\right)}{C_1 C_{T2}}} \quad \ldots(15)$$

According to given circumstances (aspect of transistor and supply voltages and bias current), simulation results show that a transconductance value of g_m=277 μA/V for the VDCC and parasitic capacitance of C_{P2}=0.92 pF and parasitic resistances of R_{P1}=43 Ω, R_{P2}=141 kΩ, R_{P3}=362 kΩ, respectively. It is seen from these parasitic values and in Eqs (14 and 15) that parasitic effects on Q′ and ω'_0 become minimum if values of g_m and G are selected bigger than G_{P2}, G_{P3}.

Considering the effects of non-ideal gains in Eq. (1) on the filter shown in Fig. 2, the output voltage V_{OUT} in Eq. (3) converts to:

$$V_{OUT} = \frac{V_2 s^2 C_1 C_2 + V_1 s\alpha C_2 g_m + V_3 \alpha\gamma_{W_N} g_m G}{s^2 C_1 C_2 + s\alpha C_2 g_m + \alpha\beta\gamma_{W_N} g_m G} \quad \ldots(16)$$

According to denominator of given non-ideal transfer function in Eq. (16), quality factor and pole frequency are obtained by:

$$Q'' = \sqrt{\frac{\beta\gamma_{WN} G C_1}{\alpha g_m C_2}} \quad \ldots(17)$$

$$\omega_0'' = \sqrt{\frac{\alpha\beta\gamma_{WN} g_m G}{C_1 C_2}} \quad \ldots(18)$$

From Eqs (17 and18), it can be observed that the tracking errors of the VDCC may cause small deviations of the values of quality factor and pole frequency. By using Eqs (17 and 18), the passive and active sensitivities of Q'' and ω''_0 can be derived in Eqs (19 and 20).

$$S_G^{Q''} = S_{C_1}^{Q''} = S_\beta^{Q''} = S_{\gamma_{W_N}}^{Q''} = -S_{g_m}^{Q''} = -S_\alpha^{Q''} = -S_{C_2}^{Q''} = \frac{1}{2},\ S_{\gamma_{W_P}}^{Q''} = 0 \quad \ldots(19)$$

$$S_\alpha^{\omega_0''} = S_\beta^{\omega''} = S_{\gamma_{W_N}}^{\omega''} = S_{g_m}^{\omega''} = S_G^{\omega''} = -S_{C_1}^{\omega''} = -S_{C_2}^{\omega''} = \frac{1}{2},\ S_{\gamma_{W_P}}^{\omega''} = 0 \quad \ldots(20)$$

It can be seen that active and passive sensitivities are equal to 0.5 in magnitude.

4 Simulation Results

Finally, a CMOS realization of a VDCC element[23] is shown in Fig. 5. The supply voltages and biasing currents are given by V_{DD}=−V_{SS}=0.9V , I_{B1}=50 μA and I_{B2}=100 μA, respectively. The aspect ratios of the

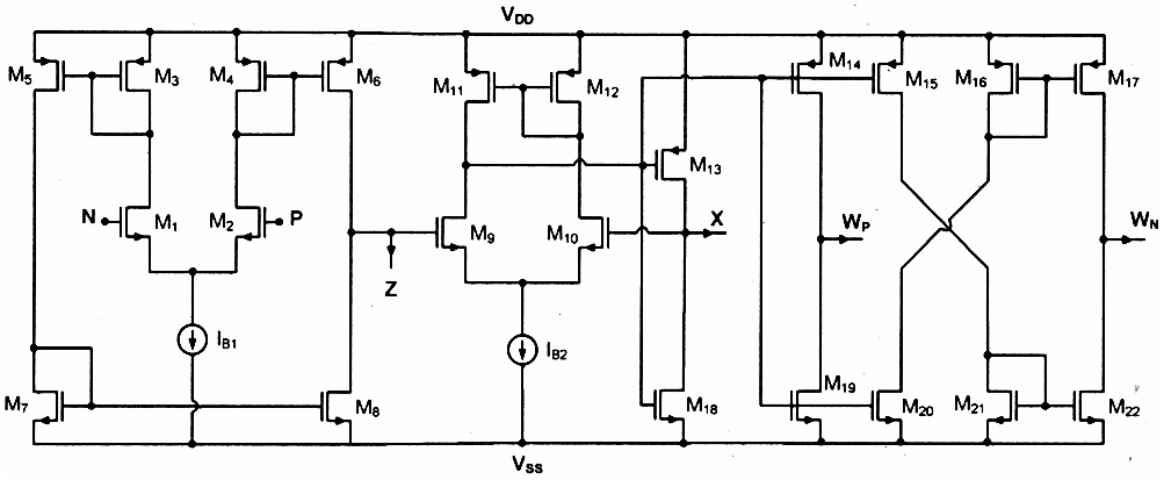

Fig. 5 — CMOS implementation[23] of the VDCC

transistors are given[23]. The MOS transistors are simulated using TSMC CMOS 0.18μm process model parameters[26].

The first voltage-mode biquad filters is shown in Fig. 5 was designed for f_0=1.165 MHz and quality factor of Q=1.34 by choosing g_m=277 μA/V, R_1=2 kΩ and C_1=C_2=50 pF. Simulation results of low-pass, band-pass, high-pass and band-stop filters are shown in Fig. 6. Gain and phase frequency responses of all-pass filter are shown in Fig. 7.

The second type SIDO voltage-mode multifunction filters are shown Fig. 3(a and b), respectively. The two SIDO voltage-mode biquad filters have been designed for f_0=1.165 MHz and Q=1.86 by choosing g_m=277 μA/V, R_1=2 kΩ, R_2=5 kΩ and C_1=C_2=50 pF. Simulation results of high-pass and band-pass filters topology is shown in Fig. 8 and 9. Figure 10 shows the simulated frequency response for the low-pass and band-pass configurations. To demonstrate the tune ability of the filter is shown in Fig. 3(b), different values of R_2 as 5, 10 and 20 kΩ are selected to obtained quality factor of 1.86, 3.72 and 7.44, respectively.

The large signal behaviour of the band-pass filter circuit of Fig. 2 is tested by applying a 1 MHz sinusoidal signal with different amplitudes to the

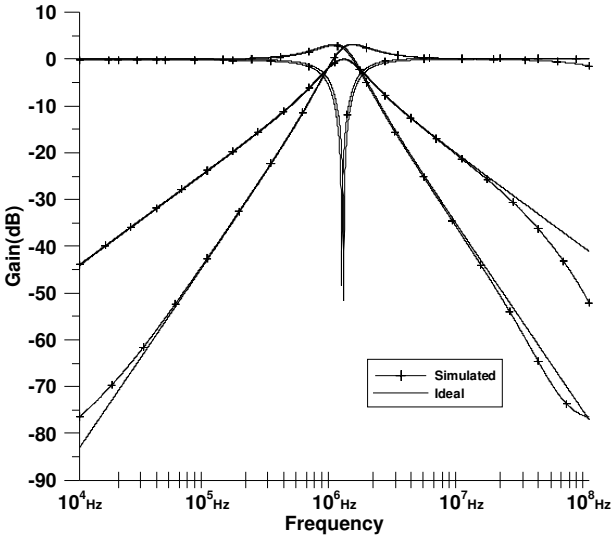

Fig. 6 — Simulated results of the gain-frequency response of Fig. 2

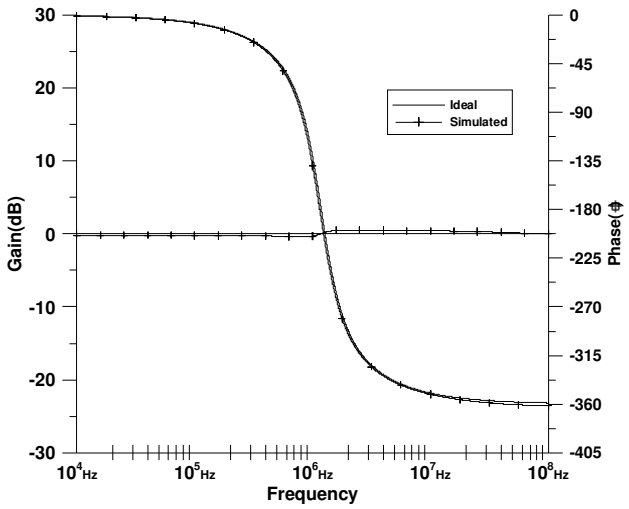

Fig. 7 — Gain and phase-frequency responses of all pass filter in Fig. 2

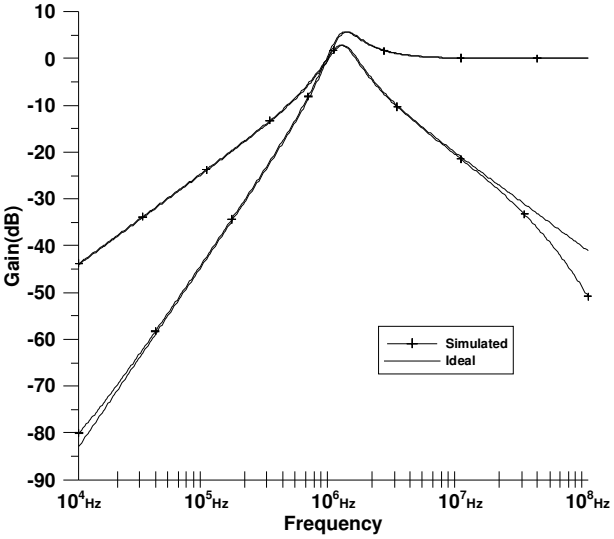

Fig. 8 — Simulated results of the gain-frequency response of Fig. 3(a)

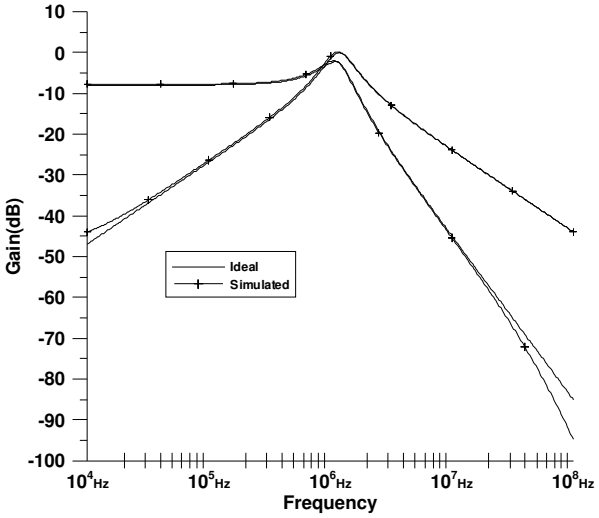

Fig. 9 — Simulated results of the gain-frequency response of Fig. 3(b)

input. The dependence of the output total harmonic distortion (THD) of band-pass filter on input voltage amplitude, which indicates the linearity of filter, is shown in Fig. 11. The harmonic distortion slowly increases depending on input voltage and for an input lower than $320mV_{p\text{-}p}$, the THD remains in acceptable limits, i.e. 3%, thus confirming the practical utility of the circuit (Fig. 11).

To determine the variation of center frequency of filter as shown in Fig. 2, depending on the all resistor and capacitor tolerance, Monte Carlo analysis was performed for 100 samples (Fig. 12). Component tolerance was considered 5% for resistors and 10% for capacitors. According to the obtained results using Monte-Carlo analysis, center frequency shift has a minimum value of 1.1197 MHz and maximum value of 1.232 MHz.

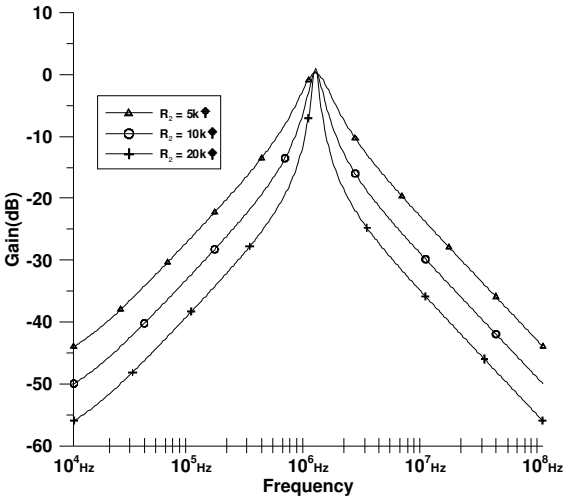

Fig. 10 — Tuning property with different values resistor of band-pass filter in Fig. 3(b)

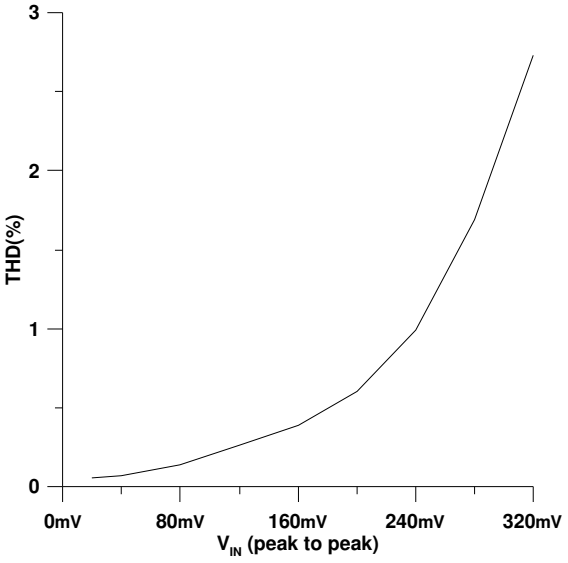

Fig. 11 — THD of the voltage-mode BP filter for an input signal at 1MHz

5 Experimental Details

To realize TISO filter, VDCC block can be generated with discrete components as shown in Fig. 13.

OPA860 integrated circuit contains the required diamond transistor (DT) or – in other words – the Current-Controlled Current Conveyor (CCCII) whose intrinsic *R*x resistance is adjustable by an external current, and, in addition, a very fast and independently utilized voltage buffer. As W_P output is not used for our filter, use of three OPA860s is enough for implementation. Here, DT_1 transistor and buffer both provide the transconductance block with *Z* output. The terminals of diamond transistor are namely *E* (emitter), *B* (base) and *C* (collector) with intrinsic resistance R_{SE} = 10 Ω of the *E* terminal. In order to increase the linearity of collector current versus input voltage, a degenerating resistor R_M which has a value of 330 Ω, is added in series to the emitter. DT_2 is a voltage follower with a low impedance output *X*.DT_3 and DT_4 provide high output impedance and dependent current sources which follow value of I_X. R_{OFFSET} is taken as 100 Ω to increase linearity, and decrease offset current between I_X-W_N and I_X-W_P output. Resistors of 100 Ω in series with the both bases of OTA and buffer inputs are connected as

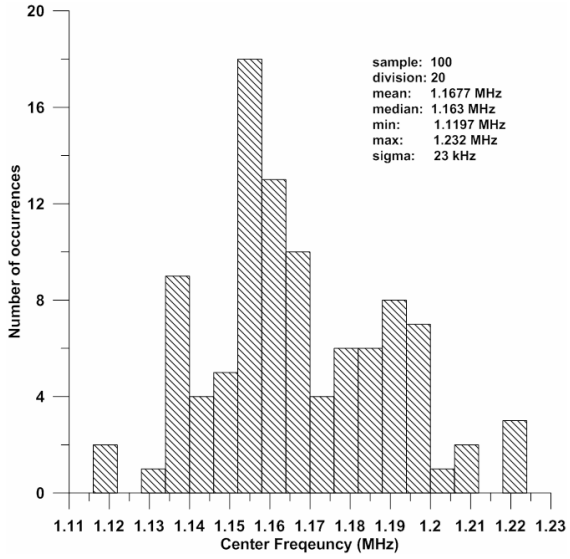

Fig. 12 — Monte Carlo analysis of center frequency shift of filter shown in Fig. 2 for 100 samples

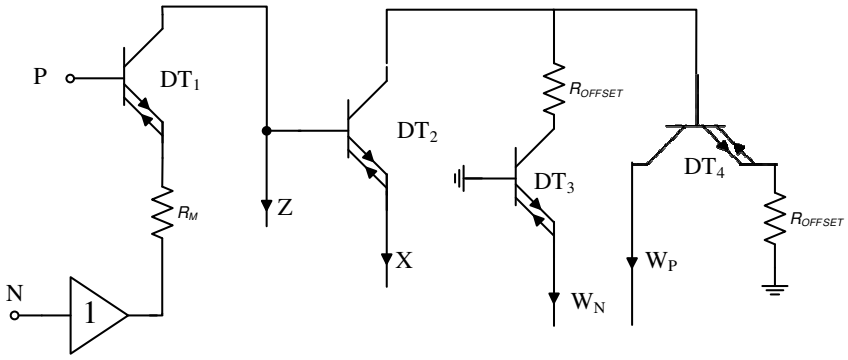

Fig. 13 — VDCC with discrete components

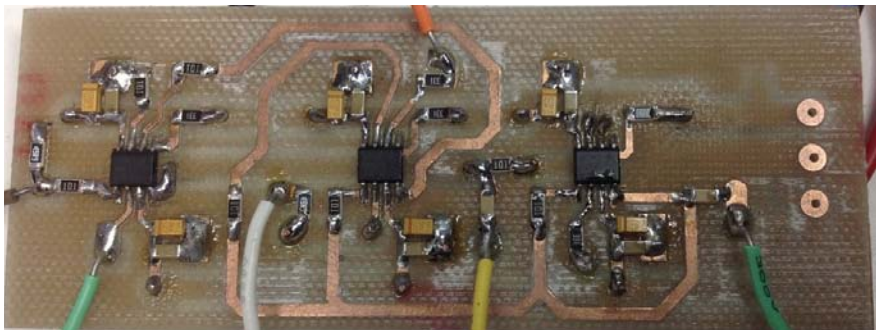

Fig. 14 — Filter circuit implemented with discrete components

recommended in datasheet[27]. These resistors help isolate trace parasitic from the inputs, reduce any tendency to oscillate, and control frequency response peaking. According to topology in Fig. 2, passive components of filter are selected as C_1=C_2=470 pF and R=$1/G$=330 Ω.

Printed circuit board of the filter is manufactured with a PCB prototyping machine (MITS Electronics) on a glass-epoxy plate with milling process. Implemented circuit using 1206 sized passive elements is shown in Fig. 14. Tantalum capacitors have a value of 2.2 µF (Kemet) and parallel with 100 nF X7R capacitors (Yageo) are added as bypass capacitors. Circuit is supplied with a dual power supply (INSTEK) at ±5 V level. Quiescent current consumption is 30 mA. To measure filter's gain and phase response, an arbitrary waveform generator (Keithley Instruments) and 2-channel digital oscilloscope are used. Output of the generator is connected to input of the filter with the internal buffer of OPA860, which has a 50 ohm parallel resistor as input to reduce output impedance of generator with impedance matching. For specific frequencies, gain and phase difference are measured by reading amplitude ratio and time-difference between output

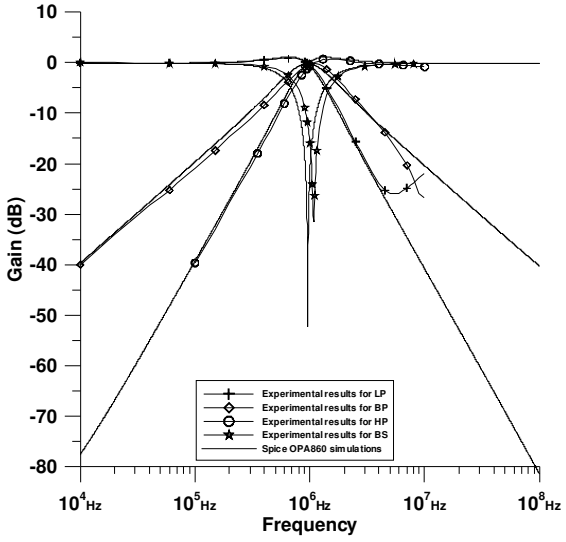

Fig. 15 — Experimental and simulation results for LP/HP/BP/BS filter

and input of the filter. For all-type of filters, experimental and simulation results are shown in Figs 15 and 16. To simulate circuit, the original SPICE model of OPA860 by Texas Instruments was used (Rev. B-Revised 4/25/06).

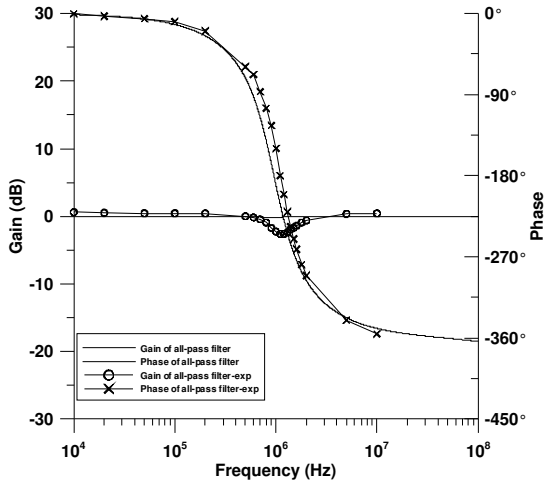

Fig. 16 — Experimental and simulation results for all-pass filter

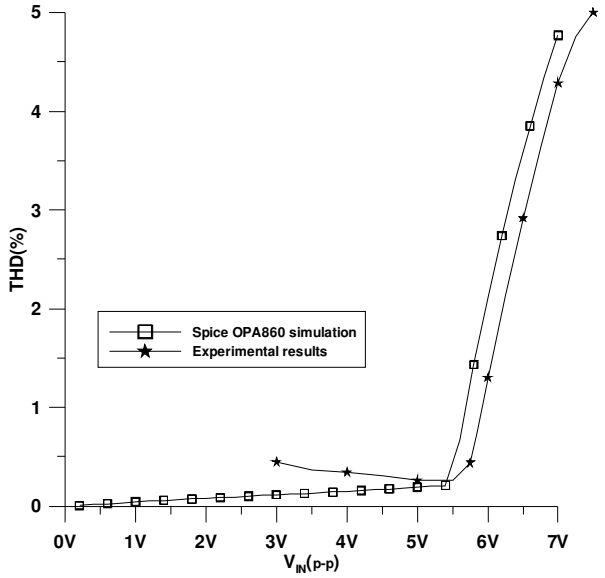

Fig. 17 — Experimental and simulation results for THD of band-pass output

For low-pass and high-pass filter structure, experimental results are nearly matched with simulation. For band-pass filter, center frequency, f_0, is measured as 1.1 MHz and quality factor is Q≈0.91as well as with simulation, f_o=957.2 kHz and Q=0.987 whereas with theoretically, f_o= 1.026 MHz and Q=1, respectively. For band-stop filter, f_o is measured as 1.08 MHz however, in simulation f_o= 957.2 kHz. By changing band-pass filter input signal level, THD is calculated by measuring amplitudes of the fundamental and harmonic signals (2^{nd} to 6^{th}) by a spectrum analyzer (INSTEK) at center frequency (Fig. 17). For input voltages under 5.9 V (p-p) level,

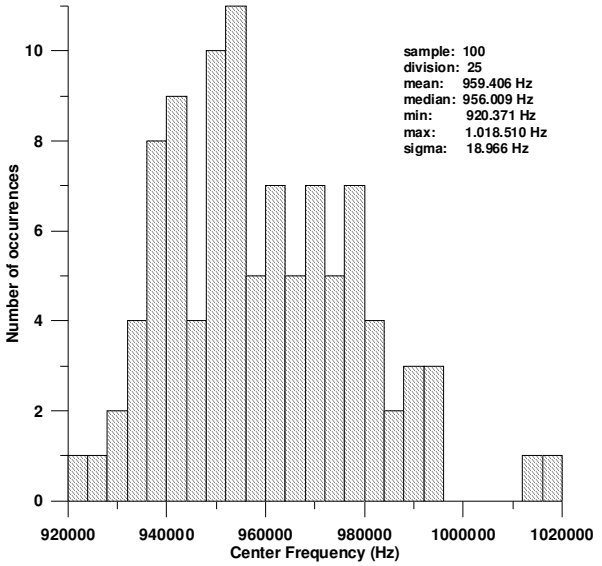

Fig. 18 — Monte Carlo analysis of center frequency shift of band-pass filter

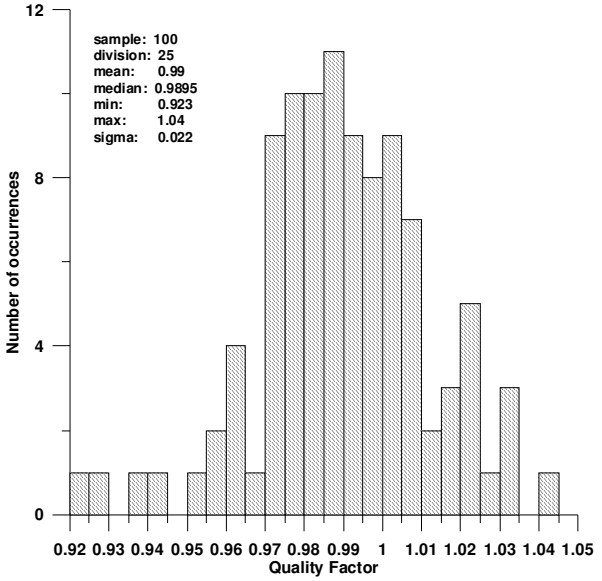

Fig. 19 — Monte Carlo analysis of quality factor shift of band-pass filter

THD of band-pass filter output is below 1%, which indicates an acceptable linearity.

To determine the variation of center frequency and quality factor of band-pass filter depending on the all resistor and capacitor tolerances, Monte Carlo analysis was performed for 100 samples and shown in Figs 18 and19. Component tolerance was considered 5% for resistors and 10% for capacitors. Center frequency shift has a minimum value of

0.92 MHz and maximum value of 1.02 MHz as shown in Fig. 18. Also, quality factor shift in Fig. 19 changes between 0.923 and 1.04.

6 Conclusions

In the present paper, three voltage mode universal biquad filters are presented. The first voltage mode filter is at three-inputs single-output multifunction filter. The other circuits are single-input dual-output filter whose quality factor can be changed by adjusting one resistor without effecting pole frequency. Also, pole frequency of all filters can be tuned electronically with changing bias current. Furthermore, all circuits require no component matching conditions so it is suitable for IC technology. Moreover, each of the circuits still enjoys low active and passive sensitivity and acceptable THD value range. We performed simulations with SPICE using 0.18 μm TSMC CMOS technology. SPICE simulation results of the filter responses are found to be in a good agreement with the predicted theory. Filter was also implemented with discrete elements using OPA860 and passive components. It is expected that the biquad filters will be useful in analog signal processing applications.

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