

## Ultra low-voltage low-power current conveyor transconductance amplifier

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This paper presents ultra low-voltage (LV) low-power (LP) CMOS structure for Current Conveyor Transconductance Amplifier (CCTA). The proposed structure is performed using recently presented technique named bulk-driven quasi-floating gate (BD-QFG) enabling the CCTA to operate at low supply voltage  $\pm 0.3$  V with low-power consumption in the micro range of 34  $\mu$ W. Moreover, the proposed circuit provides adjustable transconductance via external grounded resistor. In addition to the topology simplicity, the proposed circuit offers high linearity and extended range of transconductance controlling. Two new figure of merit (FOM) are used to characterize the performance of the design and prove its effectiveness as compared to other. Eventually, to verify the functionality of the circuit, two current mode multi-function biquad filters are included as examples of application. The simulations are performed in PSPICE environment using the 0.18  $\mu$ m CMOS n-well process from TSMC.

**Keywords:** Bulk-driven MOS, Quasi-floating-gate MOS, Low-voltage low-power, Current conveyor transconductance amplifier, Current mode filter

### 1 Introduction

Prolonging the battery life time and miniaturizing circuits are considered as basic requirements of modern portable electronics and battery-powered implantable and wearable biomedical devices. Therefore, many efforts have been exerted towards minimizing the power consumption and supply voltage of the circuits. However, circuit designers encounter difficulties to preserve reliable performance of the analog circuits with scaling down their supply voltage, owing to the fact that the threshold voltage and supply voltage are not decreased proportionally. Hence, various techniques have emerged to overcome the rather high threshold voltage problem of MOS transistors (MOSTs). Among the most effective and interesting techniques are the unconventional<sup>1-21,44-46</sup> ones, i.e. Bulk Driven (BD), Floating Gate (FG), and Quasi Floating Gate (QFG) MOST. Where the threshold voltage is significantly reduced or even removed from the signal path by using these techniques. Moreover, these techniques proved their potency to built countless LV LP active elements, such as voltage followers<sup>6,8,46</sup>, operational amplifier<sup>1,2,14,45</sup>, operational

transconductance amplifiers<sup>5,7,10,13,15,18,44</sup>, second generation current conveyors<sup>4,6,17,19</sup>, current differencing external transconductance amplifiers<sup>3</sup>, differential-input buffered and external transconductance amplifiers<sup>12</sup>, winner take all circuit<sup>9</sup>, differential voltage current conveyor<sup>20</sup>, transconductor<sup>16,21</sup> and differential difference current conveyor<sup>11</sup>.

Utilizing the BD, FG and QFG techniques offer circuit simplicity, high functionality, extended input voltage range and ultra-LV LP operation capability. However, there are some drawbacks with these techniques. Since their transconductance values are smaller than the transconductance value of the conventional gate driven (GD) MOST. As a consequence, they suffer from reduced bandwidth and higher input referred noise. On the other hand, the FG and QFG MOSTs occupy larger area on chip due to their input capacitors. Two new techniques Bulk Driven-Floating Gate (BD-FG) and Bulk Driven-Quasi Floating Gate (BD-QFG) have been revealed as promising techniques which congregate all advantages of BD and FG and QFG techniques and suppress their limitations<sup>22,43</sup>. Besides their LV LP operation capability, they enable *ac* and *dc* signals

processing. Moreover, they enjoy higher transconductance value near to the transconductance value of the GD MOST, higher bandwidth and smaller input referred noise. Recently, the implementation of BD-FG and BD-QFG MOSTs in analog circuit design shows attractive results, for instance: second generation current conveyor<sup>22</sup>, differential difference current conveyor<sup>23</sup>, transconductor<sup>24</sup>, current mirror<sup>25</sup> and voltage follower<sup>26</sup>. It is worth mentioning that BD-FG technique suffers from some limitations in comparison to BD-QFG technique, i.e. larger occupied area on the chip, uncertain residual charge trapped at the floating gate and shortage of simulation models<sup>22</sup>. Therefore, the BD-QFG has been chosen to be implemented in this work.

The Current Conveyor Transconductance Amplifier<sup>27</sup> was firstly introduced in 2005. It is considered as a versatile current mode building block for analog signal processing, which combines the advantages of the current conveyor and the operational transconductance amplifier OTA. Thus, it is expected to show the following attractive characteristics: high bandwidth, large dynamic range and high linearity. A modified version of the CCTA named Current Controlled Current Conveyor Transconductance Amplifier CCCCTA was introduced in Ref. (37). Both active elements CCCCTA and CCTA possess identical properties, except that the parasitic resistance of input terminal can be electronically controlled in CCCCTA. Although the CCTA and CCCCTA represent pure current mode active elements, they are possible to be utilized efficiently in voltage mode or hybrid mode circuits. Hence, they have widespread applicability. Numerous of analog signal processing circuits have been realized utilizing CCTA and CCCCTA, like analog signal frequency filters<sup>27-34,38</sup>, as well current mode oscillators<sup>34-36</sup>.

However, the proposed structures of the CCTA and CCCCTA in literature are not able to operate under ultra LV conditions; for instance, the supply voltage is  $\pm 1$  V in Ref. (30),  $\pm 1.25$  V in Ref. (33),  $\pm 1.5$  V in Refs (38, 39),  $\pm 1.75$  V in Ref. (32),  $\pm 1.85$  V in Ref. (29),  $\pm 2$  V in Refs (28, 34, 35), and  $\pm 10$  V in Ref. (34). Hence, the attractive performances of the CCTA cannot be exploited in ultra-LV LP applications.

In the present work, a new CMOS structure of the CCTA is realized. The proposed circuit is constructed using BD-QFG MOST. Hence, it is capable to operate

with extremely low supply voltage of only  $\pm 0.3$  V and consumes very low-power in the micro range around  $34 \mu\text{W}$ . Thus, it is very useful to be used in portable and wearable electronic equipment where the low-power dissipation is highly desired. Moreover, the proposed structure provides linear tunability of the circuit parameter. To express the efficiency of the design, relative to low-voltage working capability and extended input range, two new Figures of Merit (FOM) are presented. The first FOM<sub>1</sub> indicates the efficiency of the design regarding the threshold voltage value over supply voltage  $\text{FOM}_1 = (V_T/V_{DD}) * 100\%$ . Note that among designs with various technologies (i.e. different  $V_T$  and  $V_{DD}$ ) FOM<sub>1</sub> presents a reasonable indicator regarding the design capability of working with low-voltage supply. Second FOM<sub>2</sub> indicates the efficiency of the design regarding the maximum allowable input swing over voltage supply  $\text{FOM}_2 = (V_{in,max}/V_{DD}) * 100\%$ . Higher values of the FOM<sub>1</sub> and FOM<sub>2</sub> indicate design effectiveness. Besides, to prove operation capability, two current-mode multifunction filters based on the proposed BD-QFG CCTA circuit are introduced.

## 2 Novel ultra-LV LP BD-QFG CCTA

### 2.1 Principle of BD-QFG MOST

The BD-QFG has emerged as a promising technique for low-voltage low-power analog circuit design<sup>22,43</sup>. To demonstrate the principle of the BD-QFG technique, its symbol and the realization in MOS technology are shown in Fig. 1. It is notable that the quasi-floating gate terminal of the transistor  $M_{BD-QFG}$  is tied through a very high value resistor  $R_b$  to a suitable bias voltage on  $G_{bias}$  terminal Fig. 1(a). Practically, this resistor  $R_b$  is implemented via MOST  $M_b$  operating in cut-off region as shown in Fig. 1(b). The input voltage is applied to the quasi-floating gate through suitable capacitance from one side and to the bulk terminal from the other side.

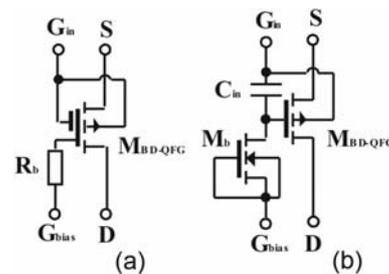


Fig. 1 — BD-QFG MOST: (a) symbol, and (b) realization in MOS technology

By utilizing the BD-QFG technique the transconductance  $g_{m,BD-QFG}$  is significantly increased as it is shown in the following equation:

$$g_{m,BD-QFG} = g_{mb} + g_{m,QFG} \quad \dots(1)$$

where  $g_{mb}$  and  $g_{m,QFG}$  are the bulk transconductance and the QFG effective transconductance, respectively. As a result, the transient frequency of the BD-QFG MOST is increased:

$$f_{T,BD-QFG} = \frac{g_{mb} + g_{m,QFG}}{2\pi(C_{bs} + C_{bsub} + C_{gs})} \quad \dots(2)$$

where  $C_{bs}$ ,  $C_{bsub}$  and  $C_{gs}$  denote bulk-source, bulk-substrate and gate-source capacitances, respectively.

**2.2 Principle of BD-QFG CCTA**

The schematic symbol of the CCTA is shown in Fig. 2. The CCTA is a five terminal active element; one low impedance input terminal (X), one high

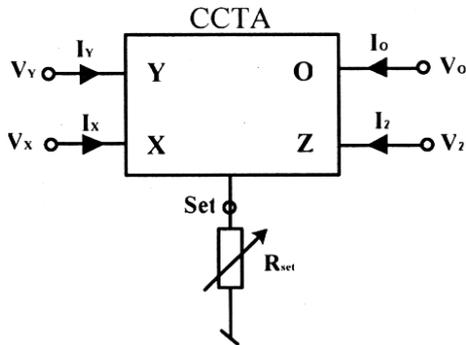


Fig. 2 — Schematic symbol of the CCTA

impedance input terminal (Y) and two high impedance output terminals (Z, O). The terminal (Set) is connected to a resistor  $R_{set}$  for tuning the effective transconductance value  $g_m$  of the circuit. The variable resistor  $R_{set}$  can be realized either by passive resistor or by voltage-controlled resistance based on simple CMOS transistor.

The input/output behaviour of the CCTA circuit can be described by the following matrix:

$$\begin{pmatrix} I_Y \\ V_X \\ I_Z \\ I_O \end{pmatrix} = \begin{pmatrix} 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & \pm g_m & 0 \end{pmatrix} \begin{pmatrix} V_Y \\ I_X \\ V_Z \\ V_O \end{pmatrix} \quad \dots (3)$$

The MOS internal structure of the proposed BD-QFG CCTA is shown in Fig. 3. The BD-QFG CCTA circuit is constructed from two BD-QFG OTAs, whereas the first OTA acts as a current conveyor and the second OTA represents a transconductor. The BD-QFG differential pairs of the first and second OTA are implemented via transistors  $M_1, M_2$  and  $M_3, M_4$ , respectively. The gates of these transistors are tied to the negative supply voltage  $V_{SS}$  through extremely high value resistors constructed by transistors  $M_{b1}, M_{b2}, M_{b3}, M_{b4}$ , respectively, which are operating in cut-off region. The input terminals of  $M_1, M_2, M_3$  and  $M_4$  are capacitively coupled via  $C_1, C_2, C_3$  and  $C_4$ , respectively to their quasi-floating gates from one side and to their bulk terminals from other side. The transistors  $M_5$  and  $M_6$  act as tail current sources of the first and the second differential pair, respectively. The multiple output current mirror

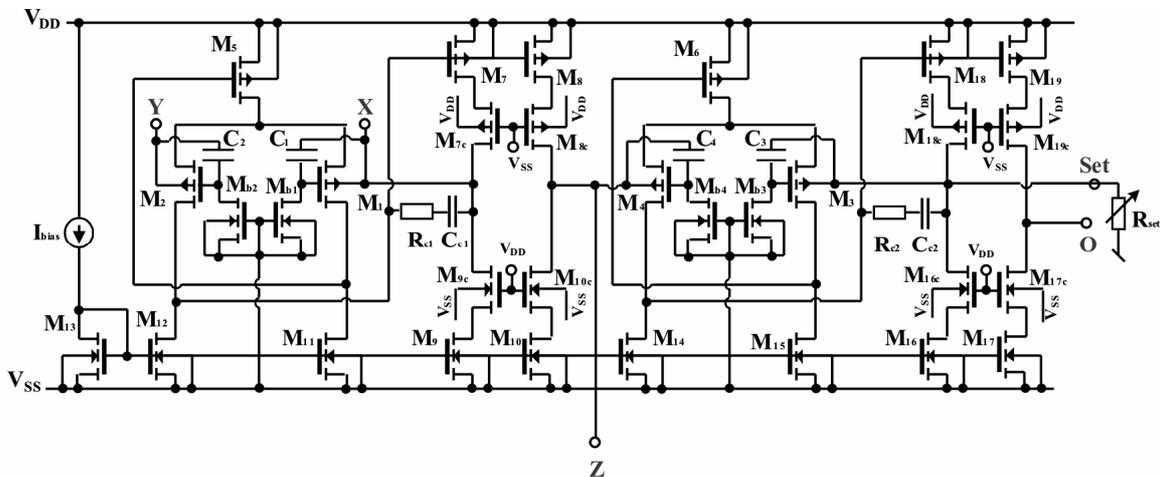


Fig. 3 — MOS internal structure of the proposed CCTA

created by transistors  $M_9, M_{10}, M_{11}, M_{12}, M_{13}, M_{14}, M_{15}, M_{16}$  and  $M_{17}$  provides current biasing of the circuit branches. The transistors  $M_7, M_{7c}, M_8, M_{8c}, M_{9c}$  and  $M_{10c}$  ensure equal currents flowing through X and Z terminals. Likewise the transistors  $M_{18}, M_{18c}, M_{19}, M_{19c}, M_{16c}$  and  $M_{17c}$  ensure equal currents flowing through O and Set terminals. The compensation networks ( $R_{c1}, C_{c1}$ ) and ( $R_{c2}, C_{c2}$ ) are implemented in the first and second OTA, respectively, to ensure the stability of the circuit. The biasing of the circuit is provided by the current bias  $I_{bias}$ . The external resistor  $R_{set}$  is used to set the value of the transconductance. Eventually, unity gain feedback is provided in the first and second OTA to confirm the voltage transfer between (X and Y), (Z and Set) terminals, respectively. Moreover, high linear controllable transconductor is obtained due to the internal feedback connection. Hence, this method of controlling the transconductance is more beneficial than the conventional method of modifying the bias current in the circuit<sup>3,21,24</sup>.

Assume that the negative feedback is disconnected and the input terminal of  $M_3$  is grounded, then the self transconductance  $g_{m,core}$  can be described by:

$$g_{m,core} = \frac{I_O}{V_Z} \quad \dots(4)$$

By reconnecting the negative feedback and the external resistor  $R_{set}$  as shown in Fig. 3, the straightforward analysis yields to:

$$V_Z - V_{R_{set}} = \frac{I_O}{g_{m,core}} \quad \dots(5)$$

$$V_Z = \frac{I_O}{g_{m,core}} + V_{R_{set}} = \frac{I_O}{g_{m,core}} + I_O R_{set} \quad \dots(6)$$

$$g_m = \frac{I_O}{V_Z} = \frac{1}{\frac{1}{g_{m,core}} + R_{set}} \approx \frac{1}{R_{set}} \text{ if } \frac{1}{g_{m,core}} \ll R_{set} \quad \dots(7)$$

The voltage transfer between X and Y can be described by:

$$\begin{aligned} \frac{V_X}{V_Y} &= \frac{g_{m,BD-QFG,M_1} r_{out1} g_{m,M_7} r_{out2}}{1 + g_{m,BD-QFG,M_2} r_{out1} g_{m,M_7} r_{out2}} \\ &\approx \frac{g_{m,BD-QFG,M_1}}{g_{m,BD-QFG,M_2}} \approx 1 \end{aligned} \quad \dots(8)$$

where  $r_{out1}$  and  $r_{out2}$  are the output impedances of the first and second stage of the first OTA as follows :

$$r_{out1} = \frac{1}{g_{o,M_2} + g_{o,M_{12}}} \quad \dots(9)$$

$$R_Z = \frac{1}{\frac{g_{o,M_8} g_{o,M_{8c}}}{g_{m,M_{8c}} + g_{mb,M_{8c}}} + \frac{g_{o,M_{10}} g_{o,M_{10c}}}{g_{m,M_{10c}} + g_{mb,M_{10c}}} + g_{o,BD-QFG,M_4}} \quad \dots(10)$$

whereas  $g_o$  is the output conductance of the correspond transistor.

The current transfer ratio is described by:

$$\frac{I_Z}{I_X} = \frac{g_{m,M_8}}{g_{m,M_7}} \approx 1 \quad \dots(11)$$

It can be observed that the minimum voltage supply required is extremely low and can be given by:

$$V_{DD,min} = V_{GS} + V_{DSsat} \quad \dots(12)$$

The cascode structure is used to provide significantly high value impedances looking into the Z and O terminals, as it can be observed from the following equations:

$$R_O = \frac{1}{\frac{g_{o,M_{17}} g_{o,M_{17c}}}{g_{m,M_{17c}} + g_{mb,M_{17c}}} + \frac{g_{o,M_{19}} g_{o,M_{19c}}}{g_{m,M_{19c}} + g_{mb,M_{19c}}}} \quad \dots(13)$$

$$R_Z = \frac{1}{\frac{g_{o,M_8} g_{o,M_{8c}}}{g_{m,M_{8c}} + g_{mb,M_{8c}}} + \frac{g_{o,M_{10}} g_{o,M_{10c}}}{g_{m,M_{10c}} + g_{mb,M_{10c}}} + g_{o,BD-QFG,M_4}} \quad \dots(14)$$

Y terminal also possess high impedance as it is expected, On the other hand, X terminal possess low impedance and it can be described by:

$$R_X = \frac{g_{o,M_2} + g_{o,M_{12}}}{g_{m,M_7} g_{m,BD-QFG,M_2}} \quad \dots(15)$$

where  $g_m$  and  $g_{mb}$  denote the gate and bulk transconductance of MOST, respectively,  $g_o$  is the transistor output conductance.

### 3 Application Examples

#### 3.1 Multiple-input and single-output (MISO) universal filter

To express that the proposed ultra-low voltage low-power CCTA can be applied to realize analog signal processing circuits, two types of universal filters using the proposed CCTA as active element are demonstrated as example applications. The first circuit is the multiple-input and single-output (MISO) universal filter as shown in Fig. 4. It employs one CCTA, two grounded capacitors  $C_1$ ,  $C_2$  and one resistor  $R_1$ . The filtering function can be obtained by appropriately connecting the input terminals.

The multiple-output Z-terminal ( $Z'$ ) and O-terminal ( $O'$ ) of CCTA can easily be obtained by adding additional current mirrors at these output terminals. Using Eq.(3), the output signal  $I_{out}$  can be obtained as:

$$I_{out} = \frac{(s^2 C_1 C_2 R_1 + s C_2 + g_m) I_{in3} - (g_m) I_{in2} - (s C_2) I_{in1}}{s^2 C_1 C_2 R_1 + s C_2 + g_m} \quad \dots(16)$$

From Eq. (16), the filtering functions can be obtained as follows:

- 1 Band-pass (BP) filter:  $I_{in1}=I_{in}$ ,  $I_{in2}=I_{in3}=0$
- 2 Low-pass filter:  $I_{in2}=I_{in}$ ,  $I_{in1}=I_{in3}=0$
- 3 High-pass (HP) filter:  $I_{in1}=I_{in2}=I_{in3}=I_{in}$
- 4 Band-reject (BR) filter:  $I_{in1}=I_{in3}=I_{in}$ ,  $I_{in2}=0$
- 5 All-pass (AP) filter:  $I_{in1}=2I_{in}$ ,  $I_{in3}=I_{in}$ ,  $I_{in2}=0$

Thus, the filter in Fig. 4 can realize all the standard types of the biquadratic filters without changing the circuit configuration as well as without active and passive-matching condition requirements. Since both two capacitors are grounded, thus the circuit is beneficial to an IC implementation<sup>41</sup>. It may be mentioned that multiple-input currents ( $I_{in}$ ) and a twice of input current ( $2I_{in}$ ) are required for realizing five standard filtering functions. In practice, the input currents  $I_{in}$  and  $2I_{in}$  can be obtained by using only an

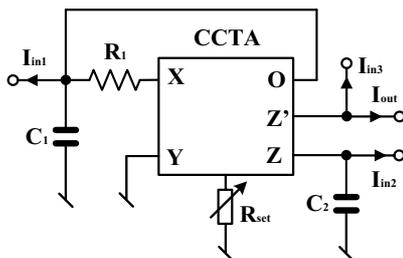


Fig. 4 — MISO universal filter using BD-QFG CCTA

additional CCTA. From Fig. 2, the input signal current ( $I_{in}$ ) is then injected into the terminal X, while each current  $I_{in}$  can be taken from terminal Z and the current  $2I_{in}$  can be taken from two Z terminals. The natural frequency ( $\omega_o$ ) and the quality factor ( $Q$ ) of Fig. 4 can be given by:

$$\omega_o = \sqrt{\frac{g_m}{C_1 C_2 R_1}} \quad \dots(17)$$

$$Q = \sqrt{\frac{C_1 R_1 g_m}{C_2}} \quad \dots(18)$$

From Eqs (17) and (18), it can be seen that the value of  $\omega_o$  for all the filter responses can be controlled by simultaneously adjusting  $g_m$  and  $R_1$  and maintaining the value of  $g_m R_1$  constant whereas the parameter  $Q$  can be controlled by simultaneously adjusting  $g_m$  and  $R_1$  and maintaining the value of  $g_m/R_1$  constant. It is further noted that the constant of values  $g_m R_1$  and  $g_m/R_1$  may easily be obtained, where the value of  $g_m$  is inversely proportional to the variable resistor  $R_{set}$ . The active and passive sensitivities of  $\omega_o$  and  $Q$  in Eqs (17) and (18) are calculated as:

$$S_{g_m}^{\omega_o} = -S_{C_1, C_2, R_1}^{\omega_o} = \frac{1}{2}$$

$$S_{C_1, R_1, g_m}^Q = -S_{C_2}^Q = \frac{1}{2}$$

#### 3.2 Single-input and multiple-output (SIMO) universal filter

The second CCTA-based universal filter is shown in Fig. 5. It is the single-input and multiple-output (SIMO) universal filter. The circuit is consisted of three CCTAs, two grounded capacitors and five grounded resistors. Using Eq. (3), the output signals  $I_{o1}$ ,  $I_{o2}$  and  $I_{o3}$  of Fig. 5 can be obtained as:

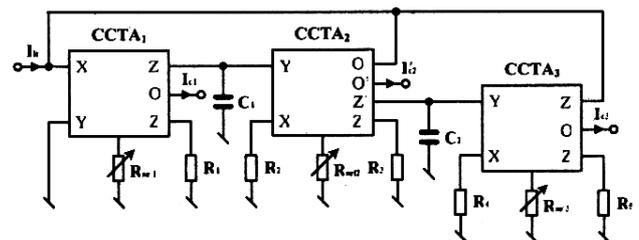


Fig. 5 — SIMO universal filter using BD-QFG CCTA

$$\frac{I_{o1}}{I_{in}} = (R_1 g_{m1}) \left( \frac{s^2 C_1 C_2 R_2}{s^2 C_1 C_2 R_2 R_4 + s C_2 R_3 R_4 g_{m2} + 1} \right) \quad \dots(19)$$

$$\frac{I_{o2}}{I_{in}} = \left( \frac{s C_2 R_3 R_4 g_{m2}}{s^2 C_1 C_2 R_2 R_4 + s C_2 R_3 R_4 g_{m2} + 1} \right) \quad \dots(20)$$

$$\frac{I_{o3}}{I_{in}} = (R_5 g_{m3}) \left( \frac{1}{s^2 C_1 C_2 R_2 R_4 + s C_2 R_3 R_4 g_{m2} + 1} \right) \quad \dots(21)$$

From Eqs (19)-(21), it can be seen that the filter simultaneously realizes the HP, BP and low-pass current response at the terminals  $I_{o1}$ ,  $I_{o2}$  and  $I_{o3}$ , respectively. Three outputs of the filter are provided through high-output impedance terminals and input is also virtually grounded which is ideal for the current-mode circuit, thus the filter in Fig. 5 is very suitable for high order filter cascade<sup>42</sup>. If BS and AP current responses are needed, BS current response can be obtained by connecting  $I_{o1}$  and  $I_{o3}$  ( $I_{o1}+I_{o3}$ ) and AP current response can be obtained by connecting  $I_{o1}$ ,  $-I_{o2}$  and  $I_{o3}$  ( $I_{o1}-I_{o2}+I_{o3}$ ). It should be noted that, for the AP response, a minus current  $I_{o2}$  ( $-I_{o2}$ ) is required. In practice, the current  $-I_{o2}$  can easily be obtained by using an additional CCTA with its y-terminal connected to ground. The current  $I_{o2}$  is then injected to the terminal x, while the minus current  $I_{o2}$  ( $-I_{o2}$ ) can be taken from the z terminal of the additional CCTA. The parameters  $\omega_o$  and  $Q$  of Fig. 5 are expressed by:

$$\omega_o = \sqrt{\frac{1}{C_1 C_2 R_2 R_4}} \quad \dots(22)$$

$$Q = \frac{1}{R_3 g_{m2}} \sqrt{\frac{C_1 R_2}{C_2 R_4}} \quad \dots(23)$$

From Eqs (22) and (23), it can be seen that the value of  $\omega_o$  for all the filter functions can be controlled by adjusting  $R_2$  and  $R_4$  simultaneously, while maintaining the value of  $R_3 g_{m2}$  constant and equaling the values of  $C_1$  and  $C_2$ . On the other hand, the parameter  $Q$  can be controlled by adjusting  $g_{m2}$  while maintaining the value of  $R_2/R_4$  constant, equaling the values of  $C_1$  and  $C_2$  and fixing the value of  $R_3$ . Therefore, the parameters  $\omega_o$  and  $Q$  can be orthogonally controlled. Moreover, the gains of HP and low-pass filter responses ( $I_{o1}$  and  $I_{o3}$ ) are adjusted by the products  $R_1 g_{m1}$  and  $R_5 g_{m3}$ , respectively. It should be mentioned that the biquadratic filter with adjustable current gain makes easy to realization sixth-order elliptic band-pass filter<sup>42</sup>. The active and passive sensitivities of  $\omega_o$  and  $Q$  in Eqs (22) and (23) are calculated as:

$$S_{C_1, C_2, R_2, R_4}^{\omega_o} = -\frac{1}{2}$$

$$S_{C_1, R_2}^Q = -S_{C_2, R_4}^Q = \frac{1}{2}$$

$$S_{R_3, g_{m2}}^Q = -1$$

The comparison between the BD-QFG CCTA-based and some previously CCTA-based filters is summarized in Table 1. It is evident from Table 1 that the proposed BD-QFG CCTA can be used to realize analog signal processing circuits. The main advantage of BD-QFG CCTA-based circuits is low-voltage

Table 1 — Comparison of BD-QFG CCTA-based filters with previously CCTA-based filters

Circuits	Type of filter	Number of active elements	Number of capacitors & resistors	All-grounded capacitor	Orthogonal control of $\omega_o$ and Q	No need matching-condition	High output impedance	Low-voltage supply and low-power consumption
This paper Fig. 4	MISO	1 CCTA	2-C & 1-R	Yes	No	Yes	Yes	Yes
This paper Fig. 5	SIMO	3 CCTAs	2-C & 5-R	Yes	Yes	Yes	Yes	Yes
Ref. (28) in 2009 Fig 2 (b)	SIMO	1 CCTA	2-C & 2-R	No	Yes	Yes	No	No
Ref. (29) in 2010	SIMO	3 CCCTAs	2-C	Yes	Yes	Yes	Yes	No
Ref. (30) in 2011	SIMO	3 CCCTAs	2-C	Yes	No	Yes	Yes	No
Ref. (31) in 2011	MISO	2 CCTAs	2-C	Yes	No	Yes	Yes	No
Ref. (32) in 2012	MISO	2 CCCTAs	2-C	Yes	Yes	Yes	Yes	No
Ref. (33) in 2013	MISO	2 CCCTAs	2-C	Yes	Yes	Yes	Yes	No

supply and low-power consumption which other previously CCTA-based circuits can be reconfigured by using BD-QFG CCTA as active elements.

**4 Simulation Results**

**4.1 Simulation results of the proposed ultra-LV LP CCTA circuit**

To prove the performances of the proposed CCTA as shown in Fig. 3, the simulations are carried out using PSPICE circuit simulation program. The LV LP CCTA circuit was employed in CMOS using 0.18  $\mu\text{m}$  CMOS process from Taiwan Semiconductor Manufacturing Company TSMC. Its PSPICE model parameters are available in Ref. 40. The optimal transistors aspect ratios of the proposed CCTA and its component values are listed in Table 2.

The simulations results of the proposed LV LP CCTA in Fig. 3 are shown in Figs 6-9. All the simulations are performed using extremely low supply voltage of  $\pm 0.3\text{ V}$  and bias current  $I_{\text{bias}}=5\ \mu\text{A}$ . The frequency responses of the current gain  $I_Z/I_X$  and voltage gain  $V_X/V_Y$  are shown in Fig. 6. The *ac* simulation of the voltage gain is performed using capacitive load of 0.1 pF. The low frequency current and voltage gains are equal to unity and the  $-3\text{dB}$  bandwidths are about 40 and 52 MHz, respectively.

Table 2 — Component values and transistors aspect ratios of the circuit shown in Fig. 3

BD-QFG CCTA	W/L [ $\mu\text{m}/\mu\text{m}$ ]
$M_1, M_2, M_3, M_4$	20/0.3
$M_{b1}, M_{b2}, M_{b3}, M_{b4}, M_9, M_{10}, M_{16}, M_{17}$	8/0.3
$M_6, M_5, M_7, M_8, M_{18}, M_{19}$	100/0.3
$M_{7c}, M_{8c}, M_{18c}, M_{19c}$	100/2
$M_{9c}, M_{10c}, M_{16c}, M_{17c}$	45/2
$M_{11}, M_{12}, M_{13}, M_{14}, M_{15}$	4/0.3
$C_1, C_2, C_3, C_4, C_{c1}, C_{c2}=0.1\text{ pF}$	
$R_{c1}, R_{c2}=3\text{ k}\Omega$	

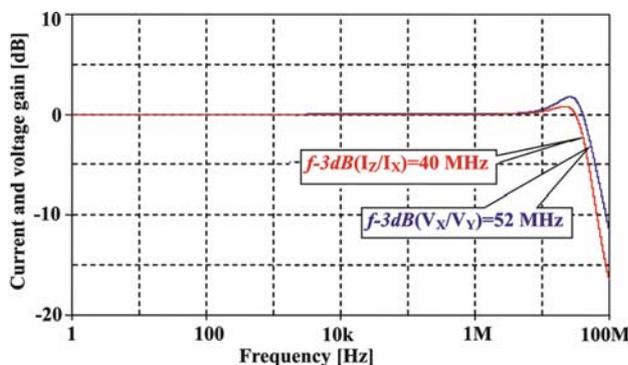


Fig. 6 — Frequency responses of the current  $I_Z/I_X$  and voltage gain  $V_X/V_Y$ .

The *dc* curves of the voltage  $V_X$  versus  $V_Y$  are shown in Fig. 7. As it can be observed, the voltage  $V_X$  follows the voltage  $V_Y$  with high linearity and wide operation range. Moreover, the voltage error is less than 2mV in the range from -250 mV to 250 mV.

The *dc* curve of the current  $I_Z$  versus  $I_X$  is shown in Fig. 8. It can be observed that  $I_Z$  follows  $I_X$  with tiny offset. The current error is less than 1.5 nA in the range from -8  $\mu\text{A}$  to 8  $\mu\text{A}$ . Actually linear operation range of  $\pm 8\ \mu\text{A}$  is suitable for ultra-low power applications, like biomedical ones.

In order to verify the transconductance  $g_m$  tunability in a wide linear range, The *dc* curves of the output current  $I_O$  versus voltage  $V_Z$  are shown in Fig. 9, with stepping  $R_{\text{set}}$  from 80 to 320 k $\Omega$  with 40 k $\Omega$  step.

The most important performance features of the proposed BD-QFG CCTA are summarized in Table 3. Based on our survey, the vast majority of the CCTA structures introduced in literature<sup>28-30,32,36,37</sup> are based on BJT, therefore, the proposed work is compared

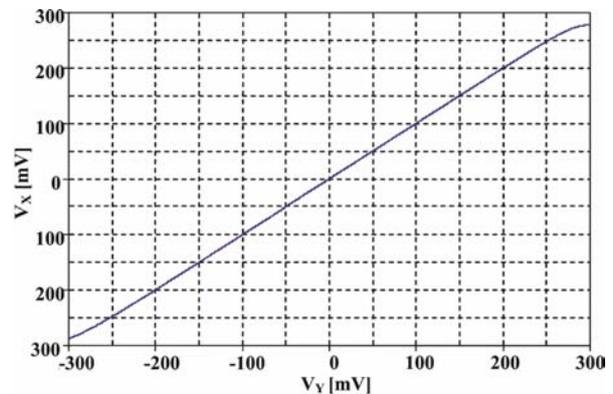


Fig. 7—DC curves  $V_X$  versus  $V_Y$  and the voltage error

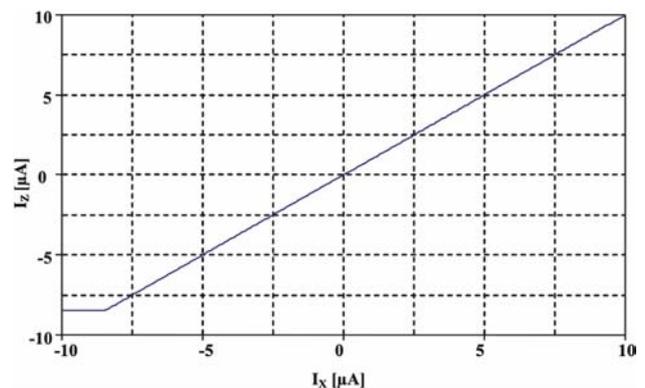


Fig. 8 — DC curves  $I_Z$  versus  $I_X$

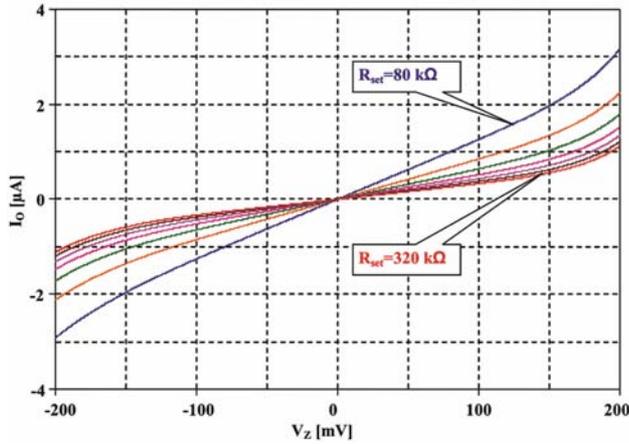

 Fig. 9 — DC curves of the output current  $I_O$  versus voltage  $V_Z$  for various values of  $R_{set}$ 

Table 3 — Performance comparison of BD-QFG CCTA with other CCTA based on GD technique

Parameters		Proposed work	Ref. (38)	Ref. (39)
Technology	( $\mu\text{m}$ )	0.18	0.35	0.35
Power supply	(V)	$\pm 0.3$	$\pm 1.5$	$\pm 1.5$
Power consumption	( $\mu\text{W}$ )	34	899	532.93
Input current linear range	( $\mu\text{A}$ )	-8.5 to 8.5	-700 to 700	$-I_{bias}$ to $I_{bias}$
Input voltage linear range	(mV)	-250 to 250	—	—
-3dB bandwidth $V_X/V_Y$	(MHz)	52	4120	495.67
-3dB bandwidth $I_Z/I_X$	(MHz)	40	333.48	1360
$g_m$ range	( $\mu\text{A}/\text{V}$ )	1-40	280-1000	4.56-250
$\text{FOM}_1 = (V_T/V_{DD}) * 100$	%	66	25	25
$\text{FOM}_2 = (V_{in,max}/V_{DD}) * 100$	%	83	—	—

with CMOS structures of CCCCTA presented in Refs (38, 39). The performances of the chosen CCCCTAs are listed in Table 3. As it has pre-stated, the simulations of the proposed BD-QFG CCTA are performed using CMOS 0.18  $\mu\text{m}$  process. On the other hand, the chosen CCCCTA circuits were simulated using CMOS 0.35  $\mu\text{m}$  process. Since each process has different threshold voltage  $V_T$  values, voltage supply requirements are also different. Hence, to provide a reasonable comparison,  $\text{FOM}_1$  and  $\text{FOM}_2$  are included in Table 3. Higher values of the  $\text{FOM}_1$  and  $\text{FOM}_2$  translate proportionate advantage in term of supply voltage and input voltage linear range. It is notable from Table 3 that  $\text{FOM}_1$  for BD-QFG CCTA is the highest, which confirms the extremely low-voltage operation capability. Unfortunately, the input dynamic ranges are not presented in Refs (38, 39),

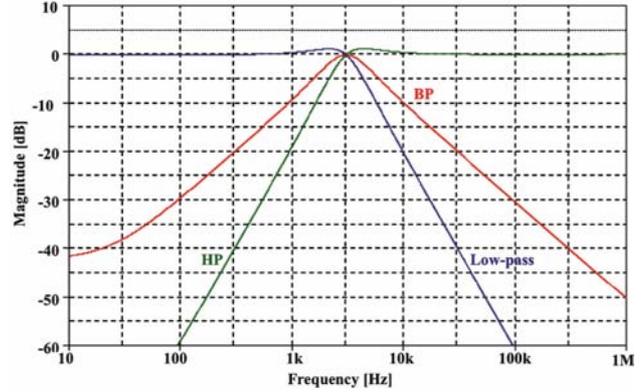
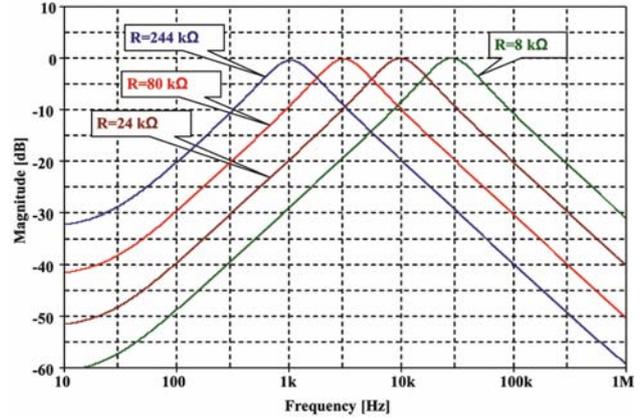


Fig. 10 — Simulated HP, BP and low-pass current frequency responses


 Fig. 11 — Simulated BP current response with variable  $\omega$ 

hence their  $\text{FOM}_2$  values could not be calculated. However, the  $\text{FOM}_2$  of our proposed circuit is 83% which is significantly high and improve the extended input dynamic range. Consequently, the effectiveness of the BD-QFG technique is proved.

#### 4.2 Simulation results of the proposed ultra-LV LP SIMO universal filter

The filter in Fig. 5 was also verified and as an example design, the capacitors  $C_1=C_2=0.65$  nF and the resistors  $R_1=R_2=R_3=R_4=R_5=R_{set1}=R_{set2}=R_{set3}=80$  k $\Omega$  are given. This setting has been designed to obtain the HP, low-pass and BP filter responses with  $f_o \cong 3.069$  kHz and  $Q \cong 1$ .

The simulated result for the HP, low-pass and BP filter characteristics is shown in Fig. 10. For this result, the natural frequency ( $f_o$ ) and the power consumption of 3.069 kHz and 123  $\mu\text{W}$  are obtained, respectively. Figure 11 shows the simulated response of the BP filter using parameter as resistors  $R$

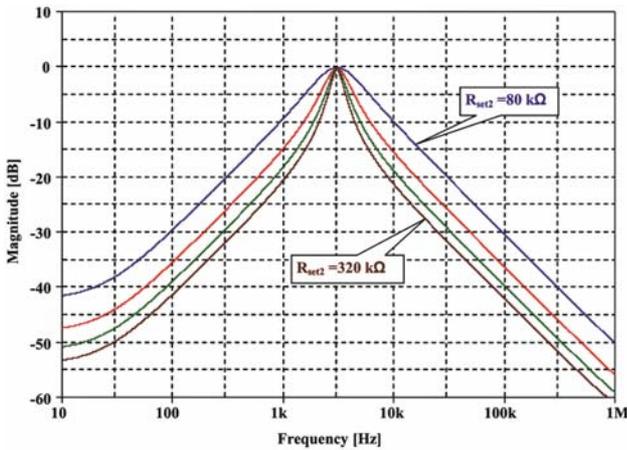


Fig. 12 — Simulated BP current response with variable  $Q$

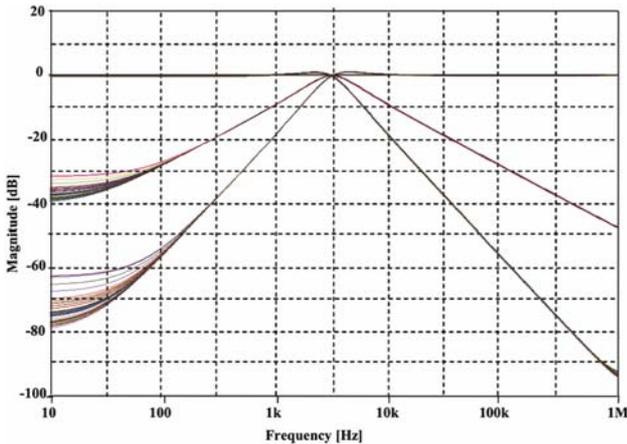


Fig. 13 — Monte Carlo simulation with 50 runs for frequency response of the proposed filter

( $R=R_2=R_4$ ) of 244, 80, 24.4 and 8 k $\Omega$ . This result is confirmed by Ref. (22). Figure 12 shows the simulated BP filter response of the proposed filter using parameter as  $R_{set2} = 80, 160, 240$  and 320 k $\Omega$ .

Monte Carlo simulation with 50 runs has been done to show the effect of 20% of the threshold variation in filter responses. The frequency responses of HP, BP and low-pass filters are shown in Fig. 13 with overlapped curves. Hence, it is clear that the effect of the threshold voltage variation is negligible.

Figure 14 shows the transient analysis of the BP filter for various temperatures (0, 27, 100) $^{\circ}\text{C}$  where sinusoidal signal with 0.5  $\mu\text{A}/3$  kHz attributes was applied to the filter input. The result confirms the functionality and efficacy of the proposed filter under various temperature conditions.

Figure 15 shows the dependence of the 3<sup>rd</sup> Intermodulation distortion (IMD) of the BP filter on

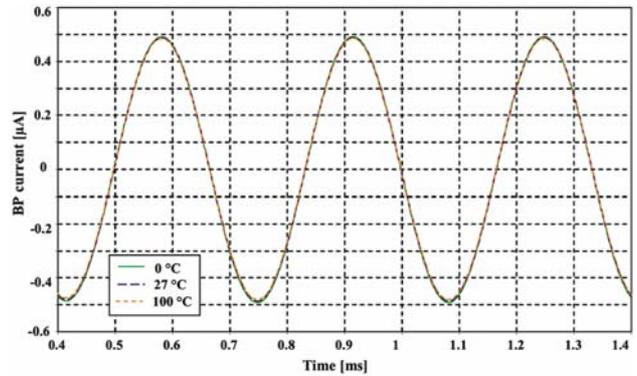


Fig. 14-Transient BP current response for various temperatures (0, 27, 100) $^{\circ}\text{C}$

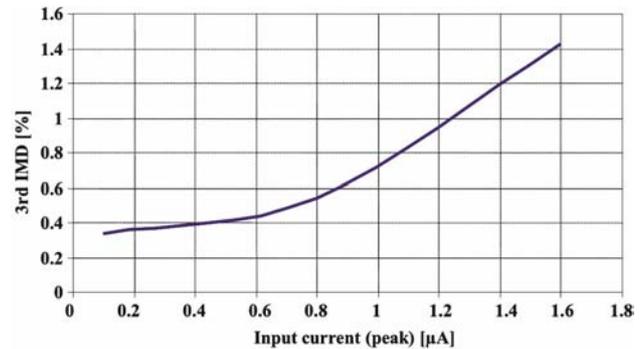


Fig. 15 — Dependence of the 3<sup>rd</sup> IMD of the BP filter on input current amplitudes

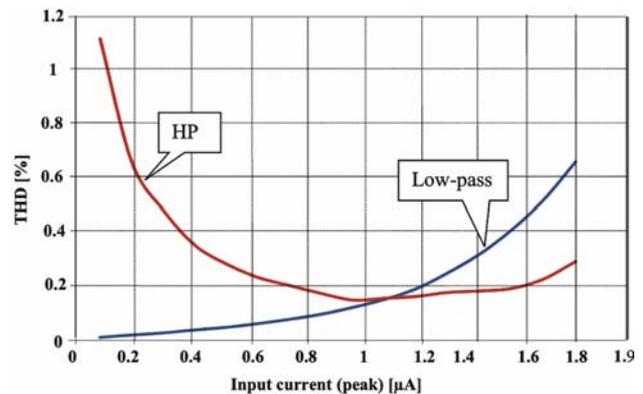


Fig. 16 — Dependence of the THD of HP and low-pass signals on input current amplitudes

two input signals amplitudes. For this purpose, two closely spaced tone of  $f_1 = 2.9$  kHz and  $f_2 = 3.1$  kHz were used with equal input signal amplitudes applied simultaneously at the input of the filter. It is evident that the 3<sup>rd</sup> IMD is below 1% for the input signals up to 1.2  $\mu\text{A}$  (peak).

The dependence of the total harmonic distortion (THD) of the HP and low-pass filters on input signal amplitude is shown in Fig. 16. The input signals have frequency of 100 Hz and 100 kHz for low-pass and HP filter, respectively. It can be observed that the THD has low values for various amplitudes.

## 5 Conclusions

The BD-QFG MOST is a very useful technique for low-voltage low-power analog circuit design, since it congregates the desired features of the conventional gate driven technique. Besides, it provides ultra-LV LP operation capability. BD-QFG technique is utilized to construct a new ultra-LV LP CCTA. Consequently, the proposed CCTA is able to operate under low supply voltage of  $\pm 0.3$  V with low-power consumption of  $34 \mu\text{W}$ . Moreover, the proposed circuit enjoys circuit simplicity, wide linear operation range and transconductance tunability. Eventually, as an example of applications a multi-function current mode filters are presented to prove the functionality of the proposed circuit. The tunable transconductance of the CCTA circuit, the quality factor and the pole frequency of the proposed filters are adjustable orthogonally.

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