



Design and Analysis of High-Performance and Low-Power Quaternary Latch, Quaternary D Flip-Flop and XY Flip-Flop

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Multiple-valued logic (MVL) circuits propose a number of possible improvements to current VLSI circuit designs. For example, serious difficulties with limitations on the number of connections between an integrated circuit and the outside world (pinout concern) and also the number of links within the circuit encountered in some VLSI circuit synthesis could be greatly reduced if signals in the circuit could assume four or more states instead of only two. This research work shows a quaternary logic-based latch, a level-sensitive flop, and an edge-sensitive flop. In most of the cases it is seen that a sequential digital circuit produces two outputs which are complementary to each other. But in most of the designs, there is no need of having both the outputs of the flip-flops, so one of the quaternary outputs can be removed from the circuit, resulting in a decrease in area and static power. In quaternary circuits, several power sources or a single power supply source are employed. Those that have several sources of supply use less energy. In multiple-valued logic we need the design to have multiple logic levels, like in quaternary logic, GND is used for logic '0', $1/3V_{dd}$ is used for logic '1', $2/3V_{dd}$ is for logic '2', and V_{dd} is for logic '3'. The multi- V_{dd} design method is incompatible with the purpose of reducing the inter-chip and intra-chip connections. In order to resolve this, a capacitive divider network is used while designing. The QFF is demonstrated with the necessary simulation results using LTSpice tool and the simulations are performed using 32nm technology file. Finally, a quaternary shift register is built to demonstrate the applicability and appropriate operation of the proposed QFF in larger sequential circuits.

Keywords: Binary logic; Multi-valued logic; CMOS; Quaternary logic; Sequential circuits; Shift register

1 Introduction

Binary logic and devices have been in use from the dawn of technology and the millennium gate design era. The development of binary logic has become arduous and time-consuming. More information may be compacted into a single figure using multivalued logic. The design and development of logic circuits has become significantly more compact and straightforward¹. Speed and power consumption are equally critical in a general VLSI system; therefore, circuit designers must consider for both². The proposed structure is far simpler and more efficient than the old one, and it can be implemented using both CMOS technology and next-generation multivalued logic devices. Some alternatives, such as ternary quantum-dot cellular automata³, quantum dot channel FETs⁴, organic anti-am bipolar transistors⁵, ZnO memristor⁶, dipole-dipole coupled proteins⁷, carbon nanotube field-effect transistors^{8,9}, and heterojunction or heterostructure transistors¹⁰, are being explored as the next-generation components for digital systems.

Latch and flops are key building blocks in sequential circuits and essential elements in digital electronics. Binary system is the most promising number system due to its simplicity and closeness to the vicinity of hardware level. Machine does not acknowledge only two numbers or logic levels *i.e.*, Logic HIGH (1) or Logic LOW (0). Binary systems are established based on the principle of Boolean Algebra, and most of the circuits in the digital world are fabricated based on the CMOS technology.

However, the main drawback of using CMOS technology is that for every logic, a complementary network of PMOS and NMOS transistors is required, which increases the area overhead of the circuit. Another major drawback is interconnection, which counts for around 70% of the chip area, and has been increasing, restricting the placement and routing of chips. Moreover, the feature size of the MOS transistor is scaling down day by day, so the CMOS technology is encountering various limitations such as heat dissipation problem, gate tunnelling, short channel effects, high leakage power dissipation and large parametric variations¹¹.

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In comparison to binary logic, quaternary logic has several advantages. It is beneficial for storing since it takes half the number of digits to store the same amount of data as the binary system; the quaternary storage mechanism is less than twice as complicated as the binary system. Quaternary logic devices, like binary logic devices, require a simpler parallel circuit to handle the same amount of data¹².

The multi-Vdd design method works against the purpose of multiple-valued logic (MVL), which is to reduce inter- and intra-chip interconnections. In research that illustrate quaternary circuits with multiple power sources, the cost of additional wirings, which impose parasitic effects and higher routing complexity, is sometimes underestimated. In contrast, quaternary systems with a single power source divide voltage to get the mid-logic values '1' and '2.' Because of the voltage divisions, a steady static current and a large quantity of static power dissipation are produced¹³.

A typical FF produces two Q and \bar{Q} outputs in simultaneously. To create the two complimentary outputs of a quaternary flip-flop (QFF) with a single power source, voltage division must occur at least twice. The more voltage division takes place, the more energy is lost¹⁴⁻¹⁶. In most of the previously discussed MVL FFs, the creation of Q and \bar{Q} is unavoidable¹⁷.

Another important feature for a circuit to be practical is its resistance to process, voltage, and temperature (PVT) fluctuations. A quaternary latch is first presented in this research. After that, it's turned into a level-sensitive quaternary flip-flop, then to an edge-sensitive quaternary flip-flop and then finally to an edge-sensitive quaternary D flip-flop (QDFF). If the intended output is not required, it allows circuit designers to delete one of the quaternary outputs, Q or \bar{Q} . The removal of \bar{Q} in the proposed QDFF, which is a single-Vdd design, results in a considerable reduction in static power¹⁸.

The flow of the paper is as follows: in Section 2, the methodology and the main ideology for designing the circuit is described and then in Section 3 a quaternary latch is designed using a capacitive divider network, which is based on single power supply. This latch has the provision to eliminate one of the quaternary outputs. A level sensitive quaternary flip-flop is then designed using this latch. This level-sensitive flip-flop is then converted to an edge-sensitive flip-flop by exploiting the master-slave concept. A new XY flip-flop is also discussed which was mainly designed to reduce the power consumption by eliminating the transistors in

the feedback path. In Section 4, a 3-bit quaternary shift-register is also designed to show the applicability of the quaternary logic in the digital world. All the simulation results are then compiled and presented in Section 5. The paper is concluded in Section 6 with all the supporting simulation values.

2 Methodology

Following key points have been considered while designing the quaternary building blocks for this work:

1. Multi-Vdd design process goes against the goal of reducing the chip connections. In order to implement different logic levels, the circuit requires to have different power supply rails. Additional wire comes at a price, resulting in parasitic effects and increased routing complexity, is often overlooked in studies that demonstrate quaternary circuits with multiple power sources. In order to implement this functionality, a potential divider network is required to take the average value of the output and to generate a quaternary value out of that¹⁹.
2. Resistive voltage dividers result in large static power consumption because of continuous static current flow in the circuit. Unlike resistors, capacitors do not squander static electricity because they function like an open circuit when completely charged. MOSCAPs are compatible with our existing CMOS based fabrication techniques and may be explored as an alternative to implement our voltage divider network. In Metal-Oxide Semiconductor Capacitor, bulk, source and drain terminals are interconnected together to act as one of the plates of the capacitor, and the gate terminal acts as the second plate. A p-type MOSCAP has a higher capacitance in comparison to an n-type MOSCAP for the same area.
3. While designing the XY flip-flop, the transistors in the feedback path are removed in order to save some more power. Also, the decoding components, such as Positive Quaternary Inverter (PQI), Negative Quaternary Inverter (NQI), and Moderate Quaternary Inverter (MQI) are also replaced by a masking layer to remove the dependency of the circuit from the variable threshold voltage values.

3 Quaternary Building Blocks

This section describes a few important quaternary building blocks which are quite versatile and extremely useful in advanced applications.

3.1 Quaternary Latch with Capacitive Divider Circuit

A basic D latch circuit is shown in Fig. 1. A binary latch is defined to have two stable states, *i.e.*, logic ‘0’ and logic ‘1’. A latch's structure always includes a loop for storing data as depicted in Fig. 1 also.

Three cross-coupled binary gates make up the proposed quaternary latch, shown in Fig. 2. The output signals (S1, S2, and S3) are reliant on the input signals (S1, S2, and S3) as well as the output values at some point in the past, where the prior time is a brief period equal to the logic gate propagation delay.

The suggested latch takes 3 times the delay value of each gate to create reliable outputs. After becoming stable, the binary outputs Q1, Q2, and Q3 produce four distinct states that may be exploited to represent quaternary digits. The final value of Q is taken after considering the average of Q1, Q2 and Q3. The simulated waveforms are shown in Fig. 3.

In digital electronics, there is often a need of resistive voltage divider networks to take the average value of the output signal. More static power is dissipated as the voltage division increases. If the desired output is not required, one pair of capacitors can be deleted to reduce static power dissipation. For representing the outputs,

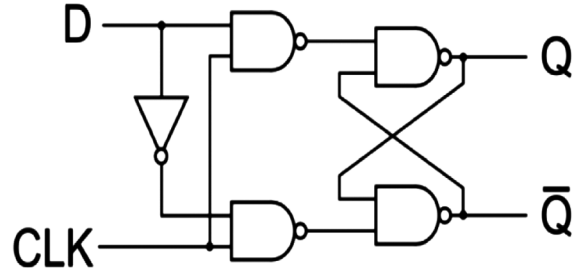


Fig. 1 — Basic NAND based D Latch Circuit²⁰.

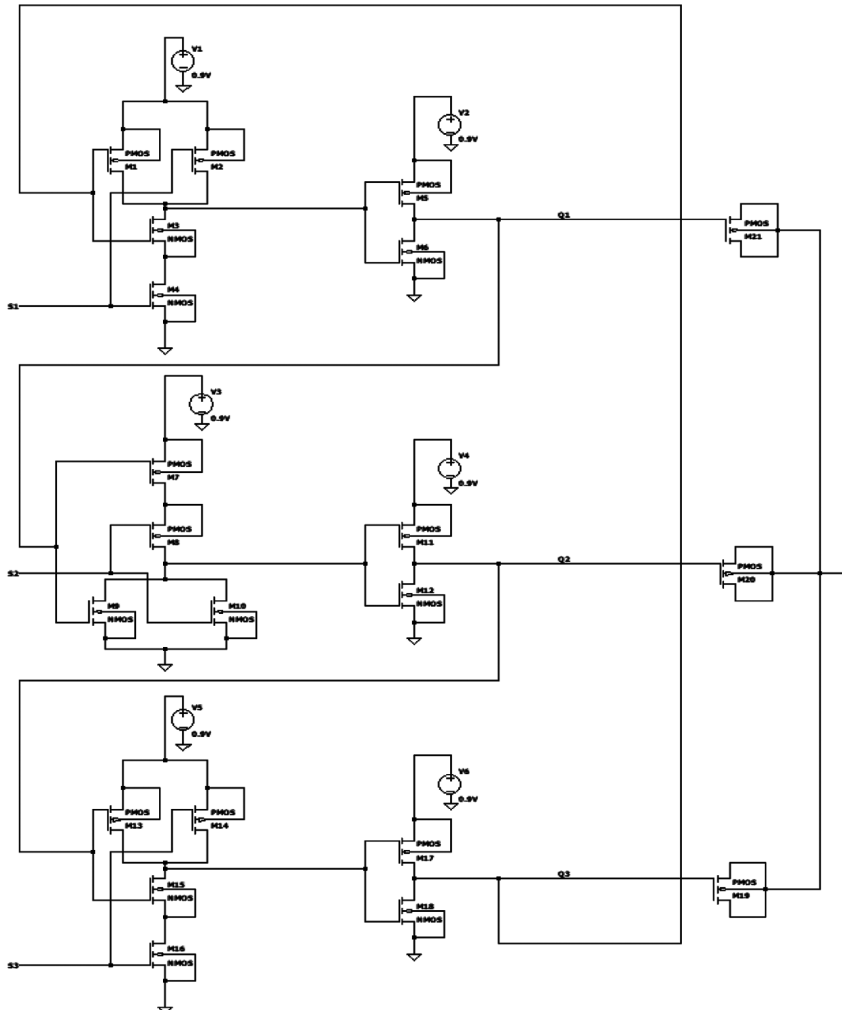


Fig. 2 — Quaternary latch - Circuit schema.

the variables used are: Q to represent normal output and \bar{Q} to represent the complemented output. There is an assumption that \bar{Q} is not an intended output, while it is possible to preserve Q while removing \bar{Q} .

$$Q=(Q1+Q2+Q3)/3 \quad \dots (1)$$

$$\bar{Q}=(\bar{Q}1+\bar{Q}2+\bar{Q}3)/3 \quad \dots (2)$$

Three-bit binary inputs S1, S2 and S3 must create eight distinct input combinations for the input, but as

per the requirement of our quaternary logic we require only four meaningful states for calculation of ‘0’, ‘1’, ‘2’ and ‘3’.

Table 1 demonstrate how the final Q output is generated depending on the previous states as well. In Table 1, Q1+t represents the next state considering a delay of t time units, Q1+2t represents the next state of Q1+t considering t units’ delay, and Q1+3t represents the next state of Q1+2t considering t units’ delay. In order to use this latch directly with any circuit, a

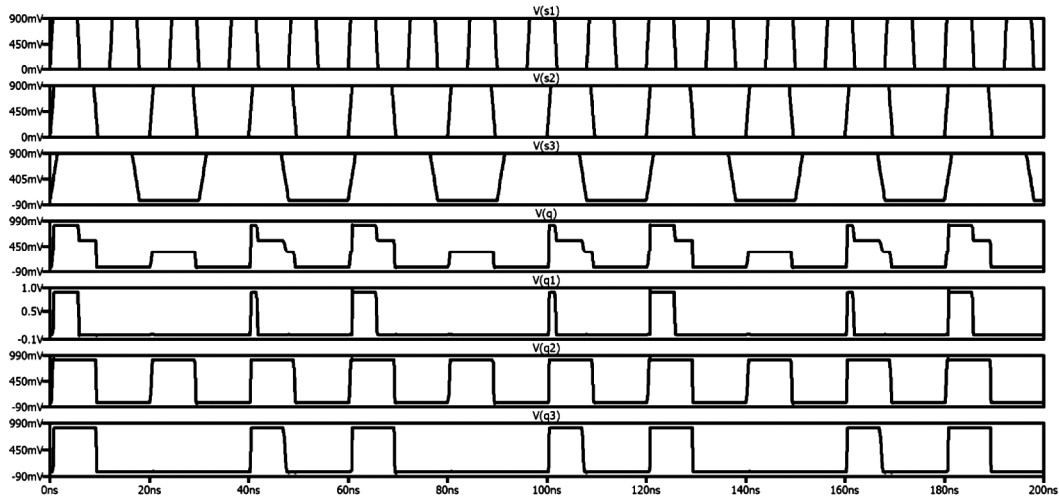


Fig. 3 — Quaternary latch – Observed waveforms.

Table 1 — Quaternary Latch – Truth Table — (Contd.)

| S1 | S2 | S3 | Q1 | Q2 | Q3 | Q1+t | Q2+t | Q3+t | Q1+2t | Q2+2t | Q3+2t | Q1+3t | Q2+3t | Q3+3t | Q Output | | |
|----|----|----|----|----|----|------|------|------|-------|-------|-------|-------|-------|-------|----------|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | |
| | | | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | |
| | | | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | |
| | | | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | |
| | | | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | |
| | | | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | |
| | | | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | |
| | | | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | |
| | | | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | | 0 |
| | | | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | | 0 |
| | | | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | | 0 |
| | | | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | | 0 |
| | | | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | | 0 |
| | | | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | | 0 |
| | | | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | | 0 |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 2 | | |
| | | | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | | | |
| | | | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | | | |
| | | | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | | | |
| | | | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | | | |

(Contd.)

Table 1 — Quaternary Latch – Truth Table — (Contd.)

| S1 | S2 | S3 | Q1 | Q2 | Q3 | Q1+t | Q2+t | Q3+t | Q1+2t | Q2+2t | Q3+2t | Q1+3t | Q2+3t | Q3+3t | Q Output |
|----|----|----|----|----|----|------|------|------|-------|-------|-------|-------|-------|-------|----------|
| | | | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | |
| | | | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | |
| | | | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | |
| 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 3 |
| | | | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | |
| | | | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | |
| | | | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | |
| | | | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | |

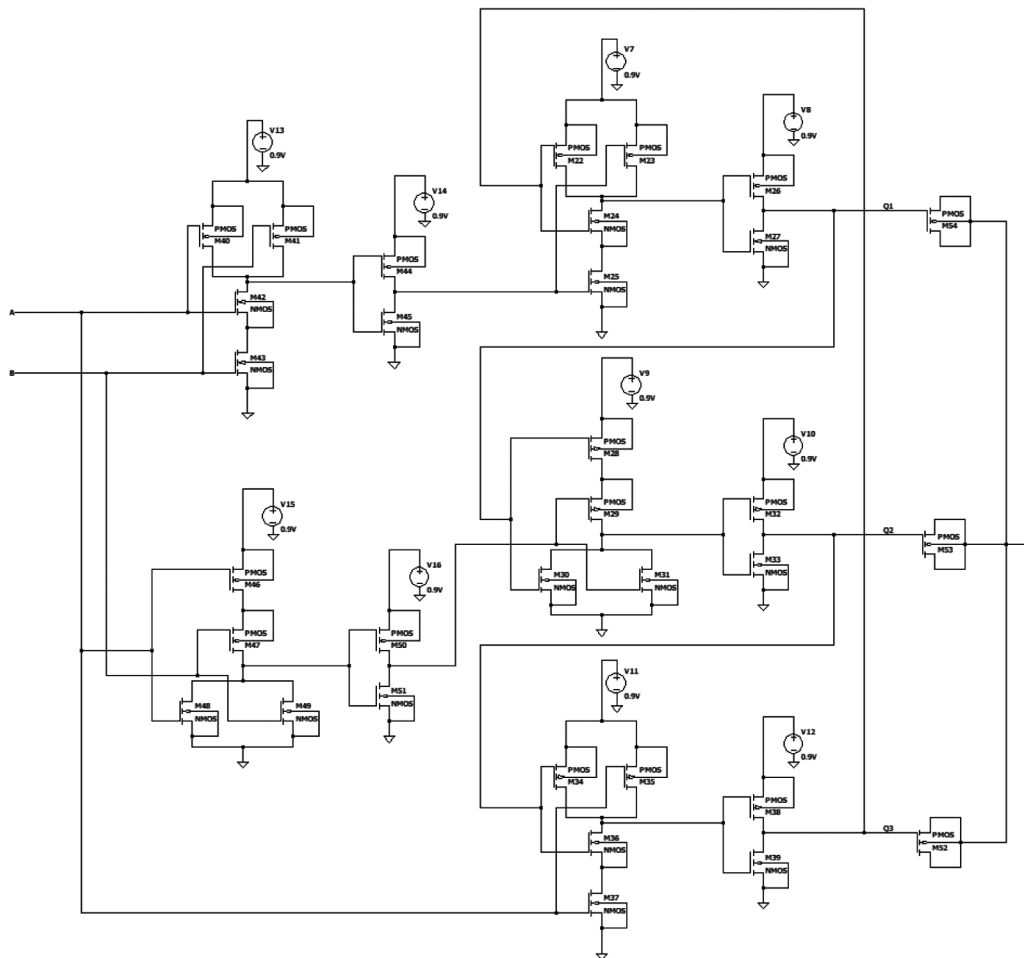


Fig. 4 — Quaternary latch incorporated with masking layer – Circuit schema.

masking layer has to be incorporated in the circuit. Since the circuit is having three inputs, so it is going to generate eight different input combinations, as per the rules of boolean algebra. There are only four meaningful states to get this circuit work properly and in order to get rid of those unmeaningful four states a masking layer is incorporated. The circuit schematic for the same is shown in Fig. 4 and the simulated waveforms are shown in Fig. 5. Table 2 has two binary inputs A and B, and two quaternary outputs Q and \bar{Q} . It can be observed

from the Table 1 and Table 2 that by adding a masking layer, four of the unwanted states can be avoided and thus the input is bound to take only the four meaningful states which are responsible for generating logic ‘0’, ‘1’, ‘2’ and ‘3’.

3.2 Positive Level-Sensitive Binary Clock based Quaternary Flip-Flop

By integrating a clock signal, the suggested quaternary latch is turned to a level-sensitive flip-flop. The sequence of events is controlled by six tri-state

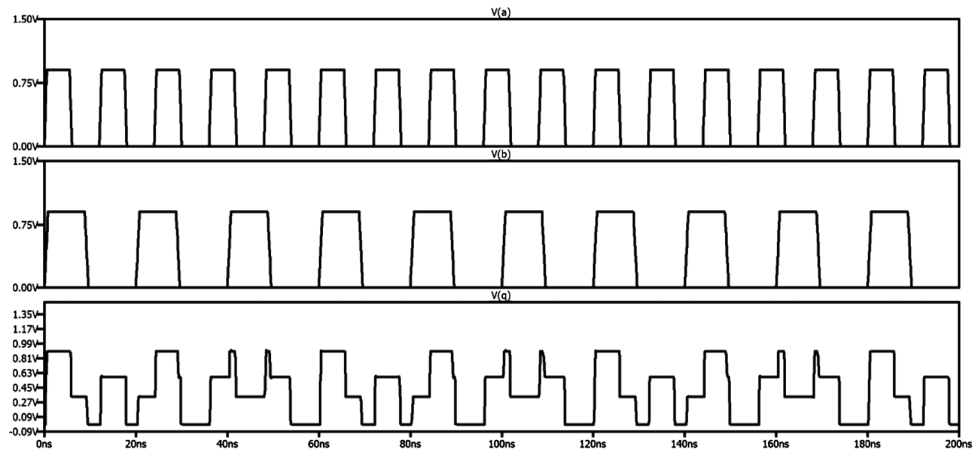


Fig. 5 — Quaternary latch incorporated with masking layer – Observed waveforms.

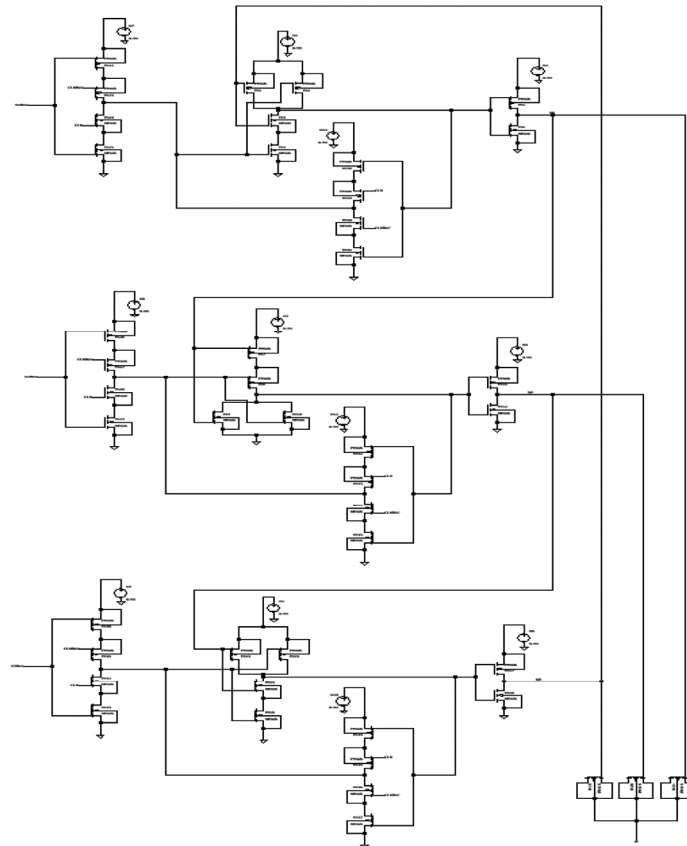


Fig. 6 — Level-sensitive QFF – Circuit Schema.

Table 2 — Quaternary latch incorporated with masking layer – Truth Table

| A | B | S1 | S2 | S3 | Q |
|---|---|----|----|----|---|
| 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 1 | 2 |
| 1 | 1 | 1 | 1 | 1 | 3 |

inverters. Three of the tri-state inverters shut off the feedback channels when CLK is HIGH, while the rest enable the inputs to set the flip-flop value. The input lines are unplugged when CLK is LOW, and the feedback paths are reconnected to retain the previous state. Fig. 6 shows the circuit schematic for level-sensitive QFF. It can be observed from the Table 3 that

the output changes its state only when the clock (CLK) signal assumes a logic HIGH value, while the last state is preserved when the CLK signal is having logic LOW value.

3.3 Positive Edge-Sensitive Binary Clock based Quaternary Flip-Flop:

Two level-sensitive QFFs are put one after the other in a master-slave design to generate an edge-

sensitive QFF. Fig. 7 shows the circuit schematic for edge-sensitive binary clock based QFF.

It can be observed from the Table 4 that the output changes its state only when the CLK signal is transitioning from LOW value to HIGH value, *i.e.*, at the rising edge of the CLK, while the last state is preserved when the CLK signal is transitioning from HIGH value to LOW value, *i.e.*, at the falling edge of the CLK.

Table 3 — Level-sensitive QFF – Truth Table

| CLK | S1 | S2 | S3 | Q1 | Q2 | Q3 | State |
|------|----|----|----|-----|-----|-----|------------|
| LOW | X | X | X | Q1- | Q2- | Q3- | Hold State |
| HIGH | 0 | 0 | 0 | 0 | 0 | 0 | Set 0 |
| HIGH | 0 | 1 | 0 | 0 | 1 | 0 | Set 1 |
| HIGH | 0 | 1 | 1 | 0 | 1 | 1 | Set 2 |
| HIGH | 1 | 1 | 1 | 1 | 1 | 1 | Set 3 |

Table 4 — Edge-sensitive QFF – Truth Table

| CLK | S1 | S2 | S3 | Q1 | Q2 | Q3 | State |
|---------|----|----|----|-----|-----|-----|------------|
| Falling | X | X | X | Q1- | Q2- | Q3- | Hold State |
| Rising | 0 | 0 | 0 | 0 | 0 | 0 | Set 0 |
| Rising | 0 | 1 | 0 | 0 | 1 | 0 | Set 1 |
| Rising | 0 | 1 | 1 | 0 | 1 | 1 | Set 2 |
| Rising | 1 | 1 | 1 | 1 | 1 | 1 | Set 3 |

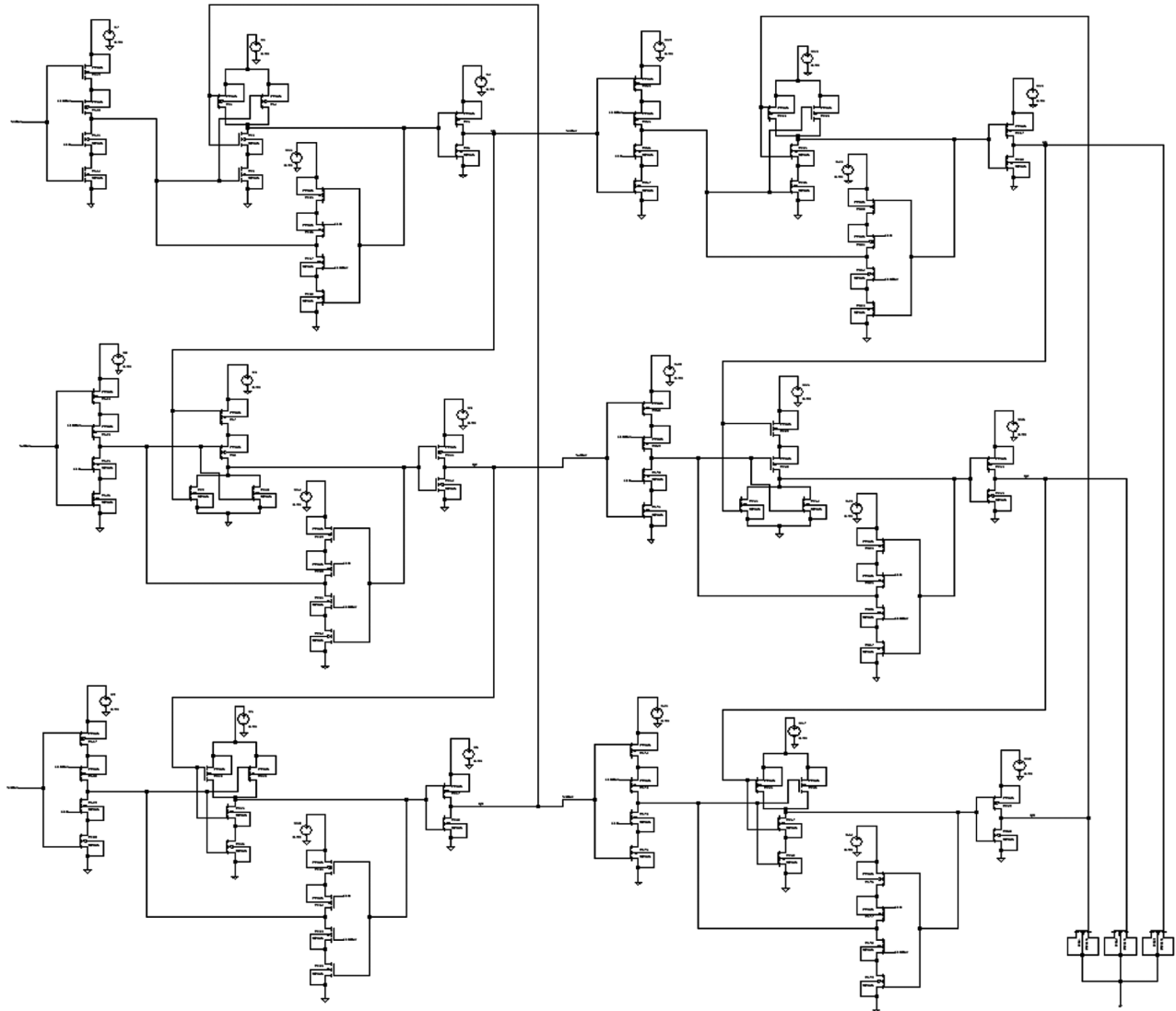


Fig. 7 — Edge-sensitive QFF – Circuit Schema.

3.4 Positive Edge-Sensitive Binary Clock based Quaternary D Flip-Flop

For the creation of each final quaternary output, three resistors are required. For the fabrication of Q and \bar{Q} , transistors are used as voltage dividers instead of resistors. There are two pass-transistors and a transmission gate in them. In single- V_{dd} MVL

circuits, transistor channel resistance is frequently used as a voltage divider. The circuit's drivability is improved by using resistive voltage dividers. The proposed circuit is entirely comprised of binary components, with voltage division taking place only at the end. Fig. 8 depicts the proposed QDFF's transistor-level construction. The majority of the

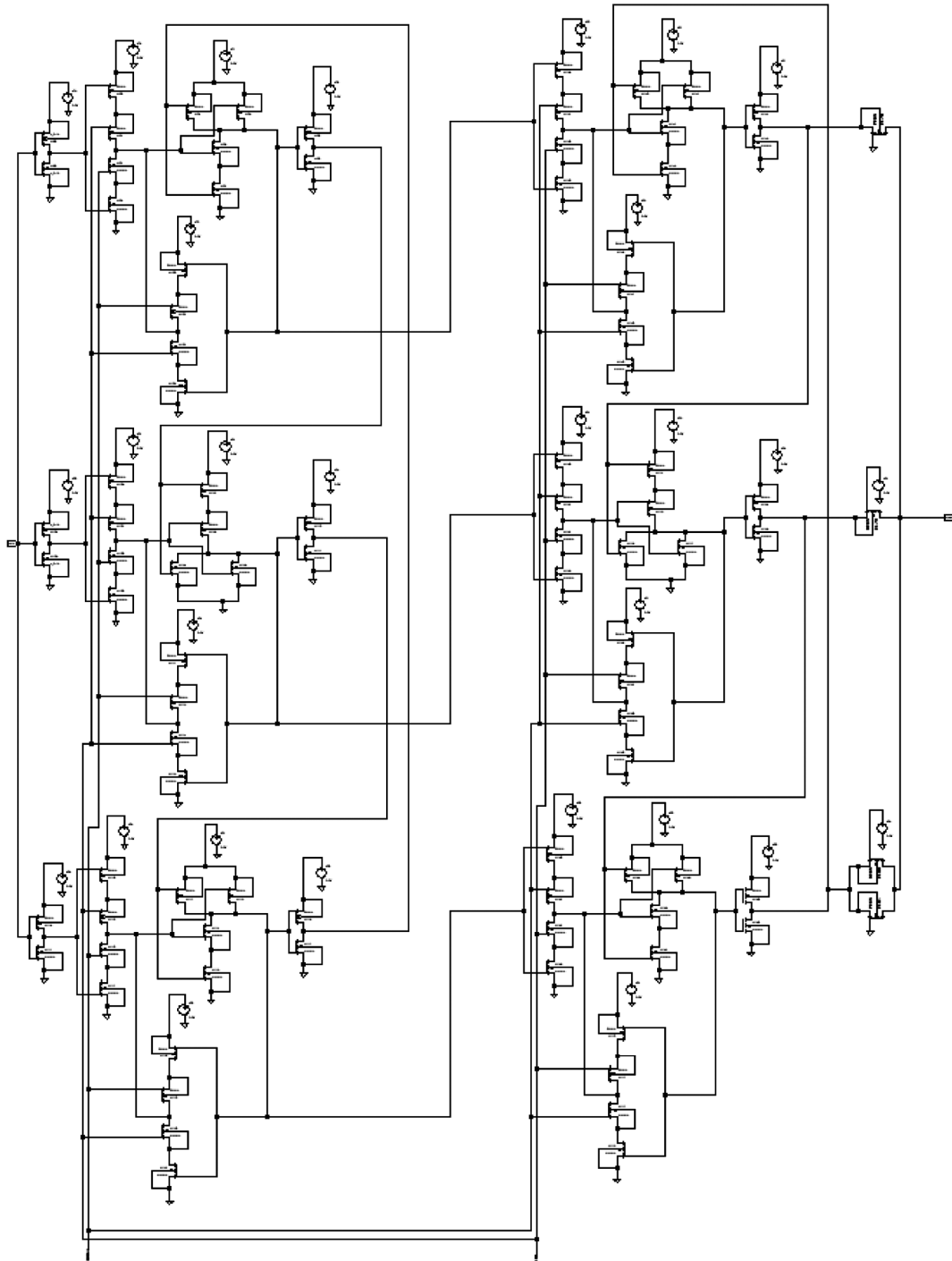


Fig. 8 — Edge-sensitive QDFF – Circuit Schema.

transistors are scaled using the standard complementary CMOS gate transistor sizing process. Fig. 9 shows the simulated waveforms for the proposed QDFF.

3.5 Positive Edge-Sensitive Binary Clock based Quaternary XY Flip-Flop:

A variety of changes are made to the QFF model to increase its performance, resulting in an improved QFF model. Six-tri-state buffers are used in the feedback path to create a state where the flip-flop can store its previous state in case of inactive clock level.

These buffers in the feedback path let the output to take some time to reach to a stable state, which is sum of the delays introduced by the buffers and the logic gates. These tri-state buffers are eliminated from the design in order to reduce the number of transistors. Fig. 10 displays the transistor structure for edge-sensitive binary clock based QXYFF. The simulated waveforms are also depicted in Fig. 11. The circuit operation for the same is explained in Table 5. As per the observation from the previous researches carried out in the domain of MVL, it is found that if the PQI, NQI and MQI decoding components are used in any circuit, then the circuit operation relies on the high and low values of threshold voltages, which in turn

decide the leakage current and the propagation delay of the circuit. Also, these different threshold voltage values are basically used to create a difference between different logic values. For instance, a threshold value of 0.5V will differentiate between 0V and 1V respective logics. Instead of using PQI, NQI and MQI, a masking layer has been incorporated into the circuit to remove the dependency of the circuit on the threshold values.

4 Application – Quaternary Shift Register (3-bit)

The transistor level structure for the shift register is shown in Fig. 12 while the simulated waveforms are shown in Fig. 13.

5 Simulation Results

All simulations have been carried out at 32nm node technology in LTSpice XVII tool. The power supply value was considered to be 0.9V. The simulations were carried out at room temperature. The observed values of the simulation are shown in Table 6. The waveforms of the circuits are also plotted along with their transistor structure, which are used to ensure that the circuits work properly. Table 7 compares the obtained power and delay for the quaternary flops based on resistive and capacitive divider networks.

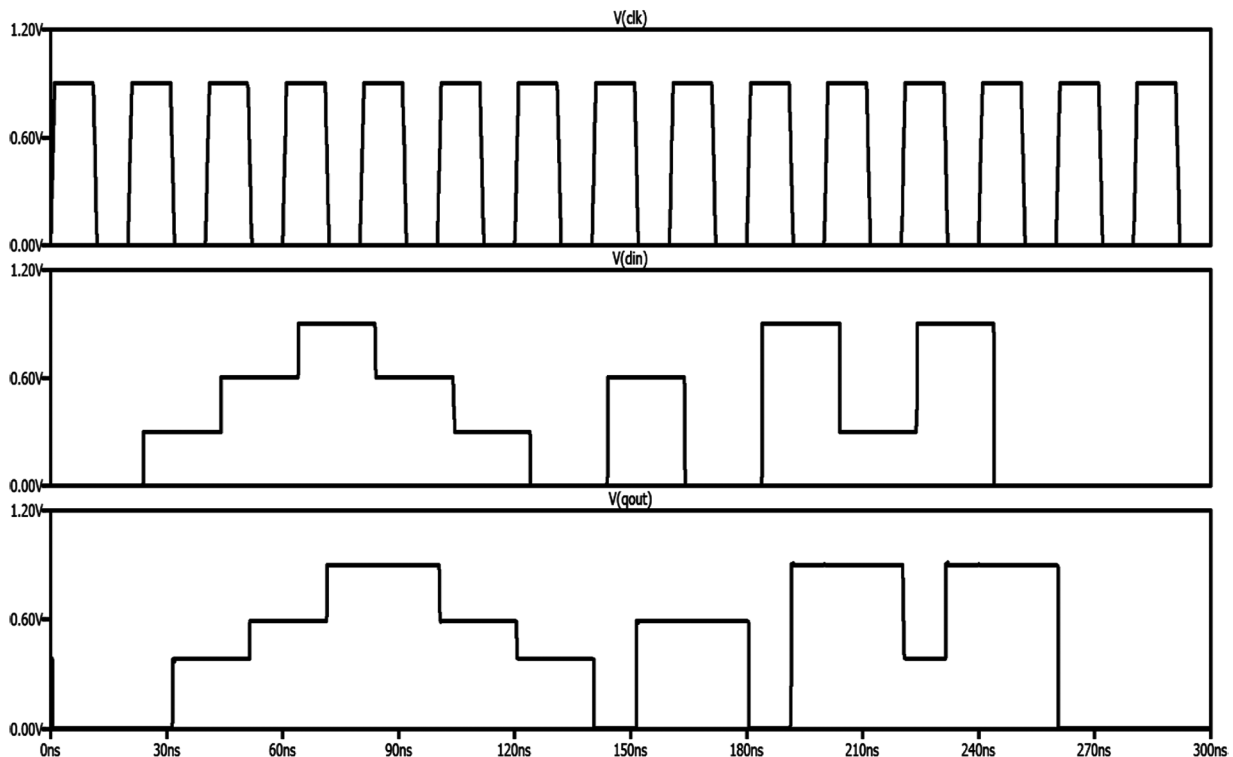


Fig. 9 — Edge-sensitive QDFF – Observed waveforms.

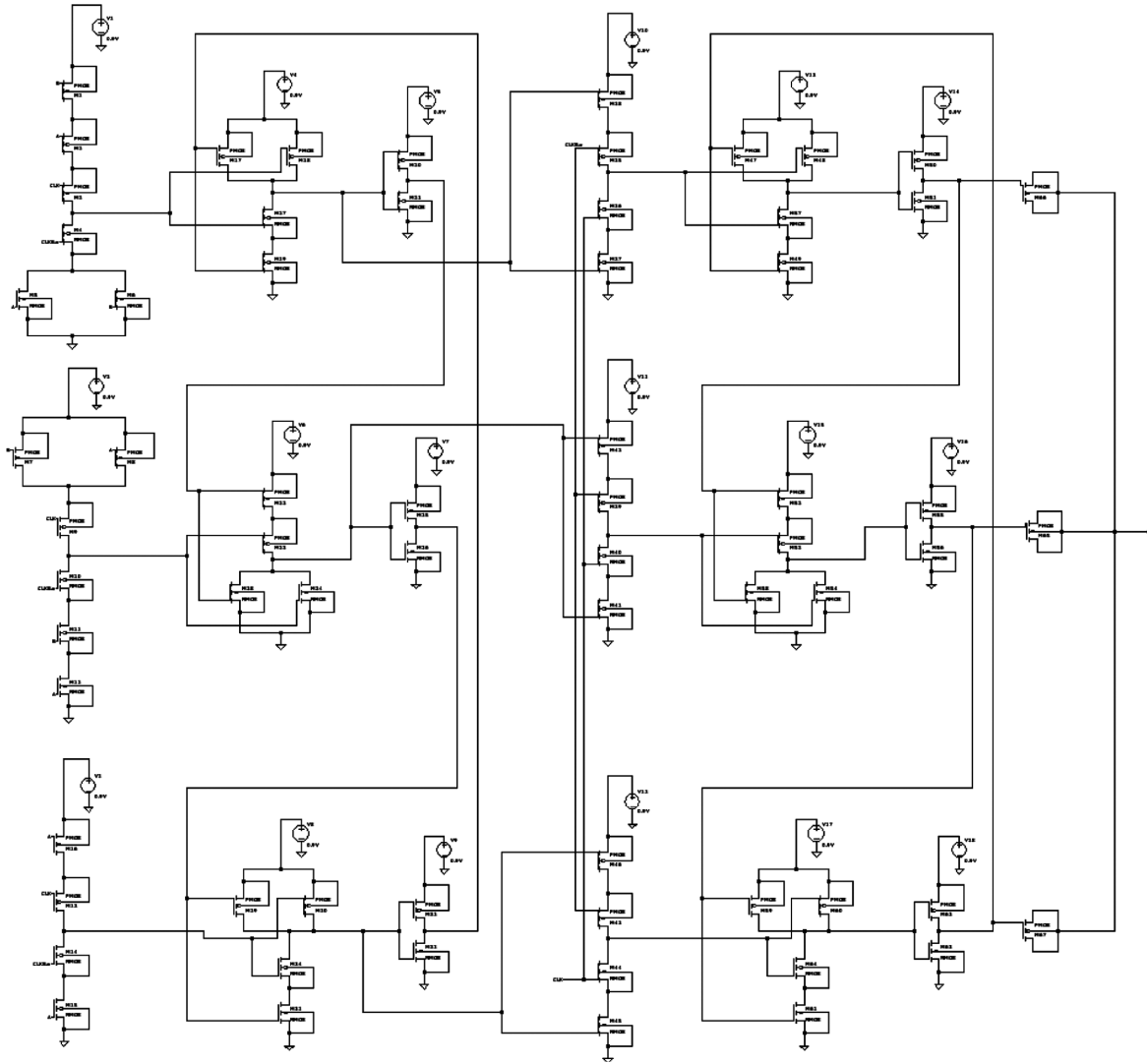


Fig. 10 — Edge-sensitive QXYFF – Circuit Schema.

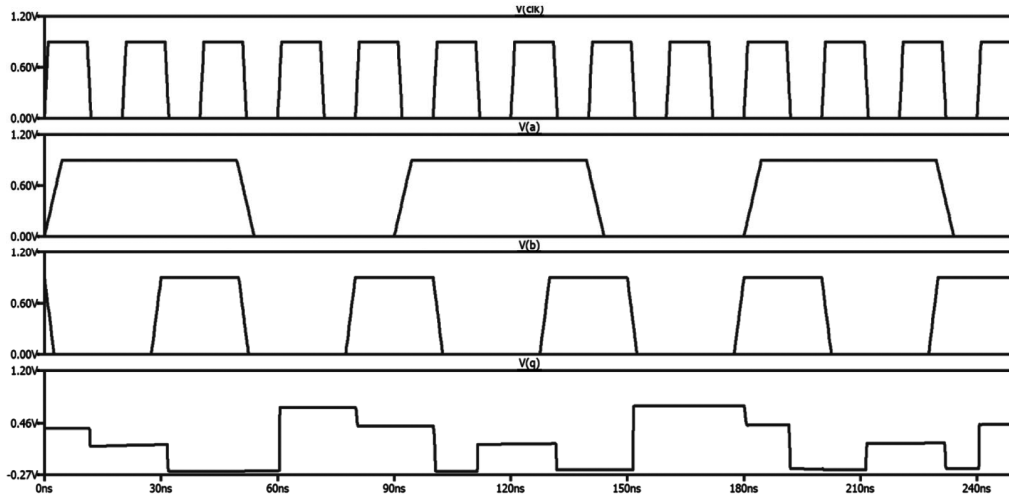


Fig. 11 — Edge-sensitive QXYFF – Observed waveform.

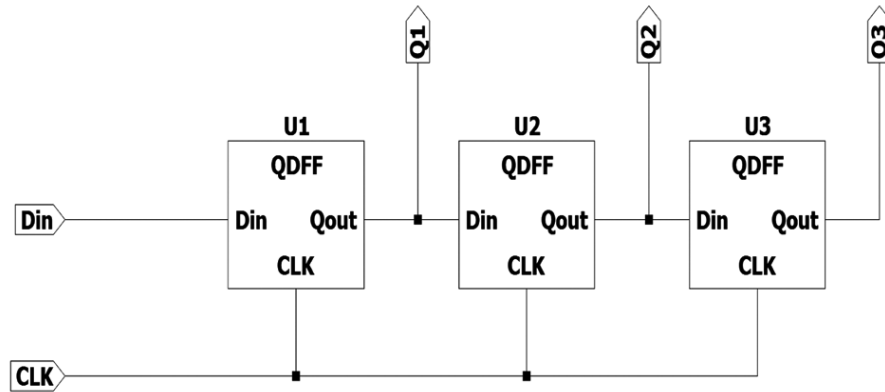


Fig. 12 — Quaternary Shift Register – Circuit Schema.

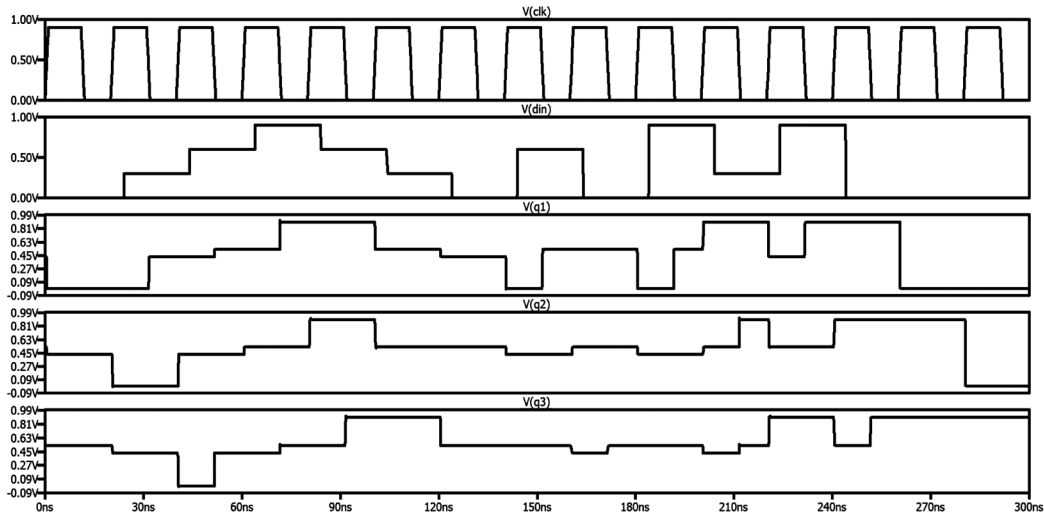


Fig. 13 — Quaternary Shift Register – Observed waveforms.

Table 5 — Edge-sensitive QXYFF – Truth Table

| CLK | X | Y | Q | State |
|---------|---|---|----|------------|
| Falling | X | X | Q- | Hold State |
| Rising | 1 | 1 | 0 | Set 0 |
| Rising | 1 | 0 | 1 | Set 1 |
| Rising | 0 | 1 | 2 | Set 2 |
| Rising | 0 | 0 | 3 | Set 3 |

Table 6 — Power and Delay Table

| Circuit | Power Consumed | Propagation Delay | | Worst Case Propagation Delay |
|-------------------------------------|----------------|-------------------|---------------------------|------------------------------|
| | | | | |
| Quaternary Latch | 21.85nW | 1.96ns | with respect to S1 input | 4.03ns |
| | | 0.165ns | with respect to S2 input | |
| | | 4.03ns | with respect to S3 input | |
| Quaternary Latch with Masking Layer | 47.16nW | 43.33ps | with respect to A input | 9.75ns |
| | | 9.75ns | with respect to B input | |
| QDFF | 612.58nW | 11.86ns | with respect to Din input | 11.86ns |
| QXYFF | 247.97nW | 43.53ns | with respect to X input | 55.53ns |
| | | 55.53ns | with respect to Y input | |
| | | 55.53ns | with respect to Din input | |
| Shift Register | 15.73μW | 28.06ns | with respect to Din input | 28.06ns |

Table 7 — Power and delay comparison

| Circuit | Power Consumed | Worst Case Propagation Delay | Power Delay Product (PDA) |
|--|----------------|------------------------------|---------------------------|
| Quaternary DFF with Capacitive Voltage Divider | 0.612 μ W | 4.03ns | 246.636 aJ |
| Quaternary DFF with Resistive Voltage Divider | 1.99 μ W | 0.176ns | 350.24 aJ |

6 Conclusion

There are two new high-performance edge-sensitive CMOS QFFs in the market. The progression from a novel quaternary latch to a novel edge-sensitive QDFF is described in detail. It allows circuit designers to choose between two quaternary complemented outputs. In MVL circuits with a single power supply, voltage division is the most common source of power consumption. Because there are fewer voltage divisions and no dispensable output, the offered customization with capacitive voltage divider network helps to decrease static power dissipation. The new designs enable a great trade-off between these two crucial features without the expense and complication of having multiple power supply, as opposed to the previously published QDFFs, which are either solely fast or low-power. The new design of XY flip-flop eliminates the extra transistors in the feedback paths and thereby consuming less power and have smaller delay as well.

References

- 1 Dhande A P & Ingole V T, *Int J Softw Eng Knowl Eng*, 15 (2005) 411.
- 2 Balla P C & Andreas A, *IEEE J Solid-State Circuits*, 19 (1984) 739.
- 3 Bajec I L, Nikolaj Z & Miha M, *Nanotechnology*, 17 (2006) 1937.
- 4 Jain F, *et al.*, *J Electron Mater*, 45 (2016) 5663.
- 5 Kobashi K, *et al.*, *Nano Lett*, 18 (2018) 4355.
- 6 Zhang Y J, *et al.*, *IEEE Trans Electron Dev*, 66 (2019) 4710.
- 7 Rakos B, *Int J Circuit Theor Appl*, 47 (2019) 1357.
- 8 Keshavarzian P & Keivan N, *Int J Nanotechnol*, 6 (2009) 942.
- 9 Lin S, Yong-Bin K & Fabrizio L, *IEEE Trans Nanotechnol*, 10 (2009) 217.
- 10 Duong N T, *et al.*, *ACS Nano*, 13 (2019) 4478.
- 11 Current K W, *Proc 30th IEEE Int Symposium on Multiple-Valued Logic*, (ISMVL), 2000.
- 12 Lang Y F & Shen J Z, *Int J Electron*, 100 (2013) 1637.
- 13 Prosser F, Wu X & Chen X, *IEE Proc E-Computers and Digital Techniques*, 135 (1988) 266.
- 14 Lang Y F, *et al.*, *Electron Lett*, 50 (2014) 1052.
- 15 Lang Y F, *Int J Electron Lett*, (2021) 1.
- 16 Datla S, Raju R P & Mitchell A T, *40th IEEE Int Symp Multiple-Valued Logic*, 2010.
- 17 Chaudhuri S, *IEEE 48th Int Symp Multiple-Valued Logic*, 2018.
- 18 Safipoor F, Reza F M & Mahdi Z, *Microelectron J*, 113 (2021) 105079.
- 19 Bolton W, *Control systems*, 2002.
- 20 Chowdary G R, *et al.*, *Int J Nanotechnol* 8 (2020).