



Design and Analysis of High-Performance and Low-Power Quaternary Latch, Quaternary D Flip-Flop and XY Flip-Flop

Mayank Shadwani* & Urvashi Bansal

Department of Electronics and Communication Engineering,
Netaji Subhas University of Technology, Sector-3 Dwarka, New Delhi-110 078, India

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Multiple-valued logic (MVL) circuits propose a number of possible improvements to current VLSI circuit designs. For example, serious difficulties with limitations on the number of connections between an integrated circuit and the outside world (pinout concern) and also the number of links within the circuit encountered in some VLSI circuit synthesis could be greatly reduced if signals in the circuit could assume four or more states instead of only two. This research work shows a quaternary logic-based latch, a level-sensitive flop, and an edge-sensitive flop. In most of the cases it is seen that a sequential digital circuit produces two outputs which are complementary to each other. But in most of the designs, there is no need of having both the outputs of the flip-flops, so one of the quaternary outputs can be removed from the circuit, resulting in a decrease in area and static power. In quaternary circuits, several power sources or a single power supply source are employed. Those that have several sources of supply use less energy. In multiple-valued logic we need the design to have multiple logic levels, like in quaternary logic, GND is used for logic '0', $1/3V_{dd}$ is used for logic '1', $2/3V_{dd}$ is for logic '2', and V_{dd} is for logic '3'. The multi- V_{dd} design method is incompatible with the purpose of reducing the inter-chip and intra-chip connections. In order to resolve this, a capacitive divider network is used while designing. The QFF is demonstrated with the necessary simulation results using LTSpice tool and the simulations are performed using 32nm technology file. Finally, a quaternary shift register is built to demonstrate the applicability and appropriate operation of the proposed QFF in larger sequential circuits.

Keywords: Binary logic; Multi-valued logic; CMOS; Quaternary logic; Sequential circuits; Shift register

1 Introduction

Binary logic and devices have been in use from the dawn of technology and the millennium gate design era. The development of binary logic has become arduous and time-consuming. More information may be compacted into a single figure using multivalued logic. The design and development of logic circuits has become significantly more compact and straightforward¹. Speed and power consumption are equally critical in a general VLSI system; therefore, circuit designers must consider for both². The proposed structure is far simpler and more efficient than the old one, and it can be implemented using both CMOS technology and next-generation multivalued logic devices. Some alternatives, such as ternary quantum-dot cellular automata³, quantum dot channel FETs⁴, organic anti-am bipolar transistors⁵, ZnO memristor⁶, dipole-dipole coupled proteins⁷, carbon nanotube field-effect transistors^{8,9}, and heterojunction or heterostructure transistors¹⁰, are being explored as the next-generation components for digital systems.

Latch and flops are key building blocks in sequential circuits and essential elements in digital electronics. Binary system is the most promising number system due to its simplicity and closeness to the vicinity of hardware level. Machine does not acknowledge only two numbers or logic levels *i.e.*, Logic HIGH (1) or Logic LOW (0). Binary systems are established based on the principle of Boolean Algebra, and most of the circuits in the digital world are fabricated based on the CMOS technology.

However, the main drawback of using CMOS technology is that for every logic, a complementary network of PMOS and NMOS transistors is required, which increases the area overhead of the circuit. Another major drawback is interconnection, which counts for around 70% of the chip area, and has been increasing, restricting the placement and routing of chips. Moreover, the feature size of the MOS transistor is scaling down day by day, so the CMOS technology is encountering various limitations such as heat dissipation problem, gate tunnelling, short channel effects, high leakage power dissipation and large parametric variations¹¹.

*Corresponding author: (E-mail: mayanks.ev20@nsut.ac.in)

Fig. 10 — Edge-sensitive QXYFF – Circuit Schema.

Fig. 11 — Edge-sensitive QXYFF – Observed waveform.

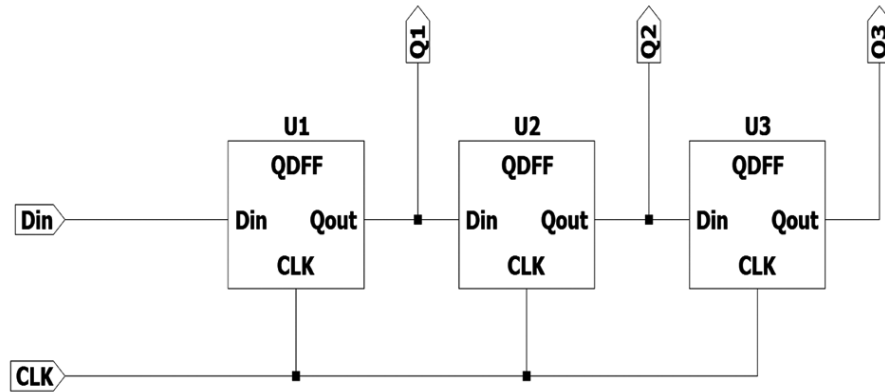


Fig. 12 — Quaternary Shift Register – Circuit Schema.

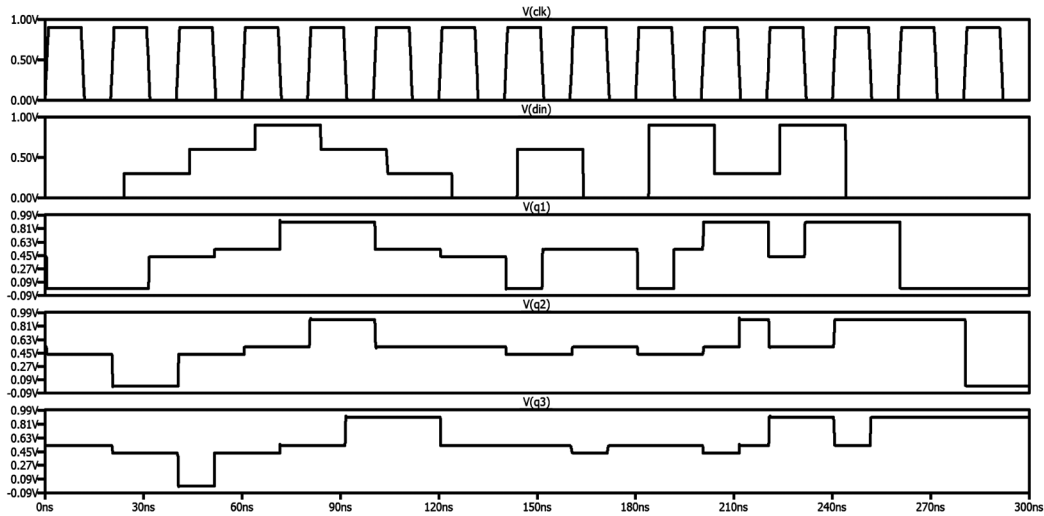


Fig. 13 — Quaternary Shift Register – Observed waveforms.

Table 5 — Edge-sensitive QXYFF – Truth Table

CLK	X	Y	Q	State
Falling	X	X	Q-	Hold State
Rising	1	1	0	Set 0
Rising	1	0	1	Set 1
Rising	0	1	2	Set 2
Rising	0	0	3	Set 3

Table 6 — Power and Delay Table

Circuit	Power Consumed	Propagation Delay		Worst Case Propagation Delay
Quaternary Latch	21.85nW	1.96ns	with respect to S1 input	4.03ns
		0.165ns	with respect to S2 input	
		4.03ns	with respect to S3 input	
Quaternary Latch with Masking Layer	47.16nW	43.33ps	with respect to A input	9.75ns
		9.75ns	with respect to B input	
QDFF	612.58nW	11.86ns	with respect to Din input	11.86ns
QXYFF	247.97nW	43.53ns	with respect to X input	55.53ns
		55.53ns	with respect to Y input	
		55.53ns	with respect to Din input	
Shift Register	15.73μW	28.06ns	with respect to Din input	28.06ns

Table 7 — Power and delay comparison

Circuit	Power Consumed	Worst Case Propagation Delay	Power Delay Product (PDA)
Quaternary DFF with Capacitive Voltage Divider	0.612 μ W	4.03ns	246.636 aJ
Quaternary DFF with Resistive Voltage Divider	1.99 μ W	0.176ns	350.24 aJ

6 Conclusion

There are two new high-performance edge-sensitive CMOS QFFs in the market. The progression from a novel quaternary latch to a novel edge-sensitive QDFF is described in detail. It allows circuit designers to choose between two quaternary complemented outputs. In MVL circuits with a single power supply, voltage division is the most common source of power consumption. Because there are fewer voltage divisions and no dispensable output, the offered customization with capacitive voltage divider network helps to decrease static power dissipation. The new designs enable a great trade-off between these two crucial features without the expense and complication of having multiple power supply, as opposed to the previously published QDFFs, which are either solely fast or low-power. The new design of XY flip-flop eliminates the extra transistors in the feedback paths and thereby consuming less power and have smaller delay as well.

References

- Dhande A P & Ingole V T, *Int J Softw Eng Knowl Eng*, 15 (2005) 411.
- Balla P C & Andreas A, *IEEE J Solid-State Circuits*, 19 (1984) 739.
- Bajec I L, Nikolaj Z & Miha M, *Nanotechnology*, 17 (2006) 1937.
- Jain F, *et al.*, *J Electron Mater*, 45 (2016) 5663.
- Kobashi K, *et al.*, *Nano Lett*, 18 (2018) 4355.
- Zhang Y J, *et al.*, *IEEE Trans Electron Dev*, 66 (2019) 4710.
- Rakos B, *Int J Circuit Theor Appl*, 47 (2019) 1357.
- Keshavarzian P & Keivan N, *Int J Nanotechnol*, 6 (2009) 942.
- Lin S, Yong-Bin K & Fabrizio L, *IEEE Trans Nanotechnol*, 10 (2009) 217.
- Duong N T, *et al.*, *ACS Nano*, 13 (2019) 4478.
- Current K W, *Proc 30th IEEE Int Symposium on Multiple-Valued Logic*, (ISMVL), 2000.
- Lang Y F & Shen J Z, *Int J Electron*, 100 (2013) 1637.
- Prosser F, Wu X & Chen X, *IEE Proc E-Computers and Digital Techniques*, 135 (1988) 266.
- Lang Y F, *et al.*, *Electron Lett*, 50 (2014) 1052.
- Lang Y F, *Int J Electron Lett*, (2021) 1.
- Datla S, Raju R P & Mitchell A T, *40th IEEE Int Symp Multiple-Valued Logic*, 2010.
- Chaudhuri S, *IEEE 48th Int Symp Multiple-Valued Logic*, 2018.
- Safipoor F, Reza F M & Mahdi Z, *Microelectron J*, 113 (2021) 105079.
- Bolton W, *Control systems*, 2002.
- Chowdary G R, *et al.*, *Int J Nanotechnol* 8 (2020).