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New Single VDCC Based Electronically Adjustable FDNR using Grounded Capacitances

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A FDNR (Frequency Dependent Negative Resistance) simulator has been presented, which uses single Voltage Differencing Current Conveyor (VDCC) along with two grounded capacitances to realize the pure FDNR function. The proposed FDNR simulator places itself as one of the most compact circuit architecture present in the available literature. It is a resistor-less realization and finds no requirement of any active/passive component/parameter matching to realize the FDNR behaviour. The presented analysis shows that the proposed circuit remains always stable under the effect of parasitics irrespective of any values of circuit parameters, which is not witnessed in many previously reported FDNRs. The usability of realized synthetic FDNR has been checked through validation of developed higher-order CDR filters by using the proposed FDNR. To verify the designed circuits, the presented configurations have been simulated under the PSPICE simulation environment. The experimental results are shown for the commercial ICs (AD844 and CA3080) based physical realization of described FDNR.

Keywords: Electronic adjustability; Frequency-Dependent Negative Resistance (FDNR); Voltage Differencing Current Conveyor (VDCC)

1 Introduction

There are an extensive number of research areas in electronics engineering where the FDNR element is found to be very useful. These fields especially include synthesis of active networks like active filters and sinusoidal oscillators, and also in cancellation of the parasitic effects in electronic circuits. Moreover, it also finds applications in quadrature oscillators, communication receivers and some other important areas of telecommunication engineering.

In the initial research work on FDNR elements, the FDNR was used to be implemented based on passive networks. Such networks found unsuitable for mono-integration due to use of passive inductors. Therefore, active elements-based FDNR simulators came into the existence and these synthetic FDNRs completely replaced the passive networks. Consequently, in literature, several actively simulated FDNRs based on different types of ABBs such as; Op-Amp (Operational Amplifier), CCII (Second Generation Current Conveyor), OTRA (Operational Trans-resistance Amplifier), CFTA (Current Follower Trans-conductance Amplifier), OFC (Operational Floating Conveyor), DVCC (Differential Voltage Current Conveyor), CFOA (Current Feedback Operational Amplifier), CBTA (Current Backward Transconductance Amplifier), CDDITA (Current Differencing Differential Input Transconductance Amplifier), VDBA (Voltage Differencing Buffered Amplifier), VDCC, VDDIBA (Voltage Differencing Differential Input Buffered Amplifier), DVCCTA (Differential Voltage Current Conveyor Trans-conductance Amplifier etc. have been reported[1-42]. The detailed comparison of the works reported in[1-42] has been shown in Table 1.

In this article, a new compact FDNR simulator has been reported employing the VDCC active element. The synthetic FDNR simulator presented in this article shows many advantages over the circuits reported in[1-42] as mentioned below;

Proposed FDNR simulator circuit requires no component matching constraint, but simulators reported[1,4, 8, 9,24,26-27,30,33-35,39-40] need matched values of passive elements or parameters of ABBs.

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Table 1 — Comparison of proposed synthetic FDNR with previously realized FDNR simulators.

Ref no.	ABB used	No. of Resistors (G (Grounded/ F(Floating))	No. of Capacitors (G/F)	Demonstration of Electronic Control (Y(Yes)/N (No))	Need of Component Matching (Y/N)	Lossless FDNR under non-ideal current/voltage transfer ratios(Y/N)	No. of CMOS/BJT Transistors
[1]	2 transcapacitance amplifiers	1 G	0	Y	Y	N	60 BJTs
[2]	3 VDTAs	0	2 G	Y	N	Y	54 CMOS
[3]	2 VDCCs	1 G	2 G	N	N	Y	56 CMOS
[4]	6 CFTAs	0	2 G	Y	Y	Y	114 MOS
[5]	2 CBTAs	1 G	2 G	Y	N	Y	68 CMOS
[6]	4 transcapacitive gyrators	4 G	8 F	Y	N	Y	18 CMOS
[7]	2 DVCCs	1 G	2 G	Y	N		36 CMOS
[8]	4 GCs	1 F	2 F	N	Y	Y	75 CMOS
[9]	4 CFOAs	1F/2G	1 F/1G	N	Y	Y	
[10]	1 DOCCII, 1 CCII+, 1 CCII-	1 G	2 G	N	N	Y	42 BJTs
[11]	1 MCFOA	1 G	1 F/1 G	N	N	Y	32 MOS
[12]	2DO-CCCIIs, 3 CCII+s	2 G	2 G	N	N	Y	56 BJTs
[13]	2 CCIIs, 1 INIC	1 F	2 F	N	N	Y	24 BJTs
[14]	2 CCI	3 F	2 F	N	N	Y	12 BJTs
[15]	1 DVCC, 3 CCIIs	3 G	2 G	N	N	Y	49 BJTs
[16]	2 DVCCTA	1 G	2 G	Y	N	Y	27 BJTs
[17]	2 DVCCIIs	1 G	2 G	N	N	Y	36 MOS
[18]	2 DOCCIIs	1 G	1 F/1 G	N	N	Y	48 BJTs
[19]	5 CCIIs	2F/1G	2 G	N	N	Y	60 BJTs
[20]	4 CCIIs	2 G	2 F	N	N	Y	48 BJTs
[21]	1 VDTRA (1 DVCC, 1 OTA and 1 DO-CCII)	0	2G	Y	N	Y	56 CMOS
[22]	3 CCCII+s	0	2 G	N	N	N	
[23]	1OTRA	2 F	3 F	N	N	Y	
[24]	2 CDDITAs	0	1F/1G	N	Y	N	78 CMOS
[25]	2 VDDIBAs	1 F	1F/1G	N	N	Y	56 CMOS
[26]	1 ZC-VDTA (non-ideal FDNR)	0	2 G	Y	Y	N	24 CMOS
[27]	1 OTRA	2 F	2 F	N	Y	Y	
[28]	2 VDBAs	2 F	1 F	Y	N	Y	22 BJTs
[29]	2 OFCs	2 G	1 G	N	N	Y	
[30]	2 transconductance amplifiers	0	2 G	N	Y	Y	16 CMOS
[31]	2 VDCCs	1 G	2 G	Y	N	Y	56 CMOS
[32]	5 Gm Cell	0	2 G	Y	N	Y	40 CMOS
[33]	1 CFOA	1 F/2F	1 F/2 G	N	Y	Y	1 AD844
[34]	1 DVCVS/DVCC, Diff. Buff. Amp	1 F	2 G	N	Y	N	
[35]	4 OP AMPs	1 F	0	N	Y	Y	
[36]	4 CCIIs	3 G	2 G	N	N	Y	4 AD844s
[37]	2 CCIIs	3 F	1 F/2 G	N	N	Y	2 AD844s
[38]	3 OP AMPs, 1 FET	1F/1 G	2 F	N	N	Y	
[39]	1 OP AMP	1 F/2 G	2 G/1F	N	Y	Y	
[40]	1 CCs	2 F/2 G	1 F/1 G	N	Y	Y	
[41]	1 DIBTA (3 AD844s)	0	2 G	N	N	Y	3 AD844
[42]	1 FDCCII	1 G	2 G	N	Y	Y	
Proposed	1 VDCC	0	2G	Y	N	Y	22 CMOS

In the designed circuit, the value of FDNR can be changed by varying the biasing currents of VDCC, while the FDNRs reported[1,2,4-7,16, 21, 26, 28, 31,32] have no feature of electronic controllability.

The proposed circuit uses only a single VDCC to realize the FDNR simulator, while the configurations reported[1-10,12-20, 22,24-25,28-32,34-38] require two or more ABBs, therefore the proposed simulator can be considered as a compact structure as compared to so many previously reported FDNR simulators.

The proposed configuration is purely a resistor-less realization while FDNR simulators reported[1,3-20,23,25, 27-29, 31,33-40,42] employ one or more external resistors. Also from the viewpoint of total number of employed passive elements the proposed circuit structure is found better than many previously reported configurations as it employs only two passive elements.

The presented circuit employs passive element in floating state (both the capacitances are grounded), while the simulators given [6,8-9,11,13-14,18-20,23-25, 27-28,33-35,37-40] requires at least one floating element. Therefore, the proposed simulator is suitable for monolithic integration.

It can also be witnessed that some previously reported configurations [1,22,24,26,34] do not realize the pure FDNR functions unlike the proposed one, which simulates the pure FDNR function with no lossy term.

2 Proposed Configuration

The circuit idea of the VDCC was first reported in[43] as a modern ABB for analogue circuit designing. Since then various analog signal generations circuits, signal processing circuits, and impedance simulation circuits employing VDCC components have been designed and reported in the literature[44-46]. The single block representation of the VDCC block is depicted in Fig. 1 and its CMOS implementation is shown in Fig. 2[47]. In Fig. 2 the inputs are denoted as p and n while the output terminals are represented as z, x+, and x-. The terminal relationships of VDCC can be described by the matrix shown in equation (1).

$$\begin{bmatrix} I_X \\ I_Y \\ V_X \\ I_Z \\ I_{0+} \\ I_{0-} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ \alpha & 0 & 0 \\ 0 & -\beta & 0 \\ 0 & 0 & \gamma g_m \\ 0 & 0 & -\gamma g_m \end{bmatrix} \begin{bmatrix} V_Y \\ I_W \\ V_Z \end{bmatrix} \quad \text{... (1)}$$

For the balanced output OTA (M_1-M_8), the transconductance gain (g_m) of the VDCC can be defined as:

$$g_m = \sqrt{K_n \left(\frac{W}{L}\right) I_{B1}} \quad \text{... (2)}$$

where, $K_n = \mu_n C_{ox}$ is the transconductance parameter, (W/L) is the ratio of the width-to-length of the

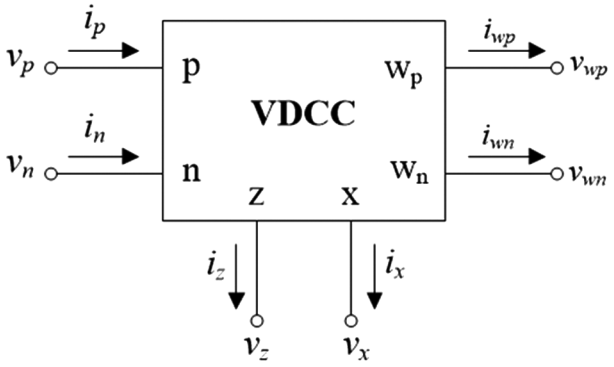

Fig. 1 — Block portrayal of VDCC

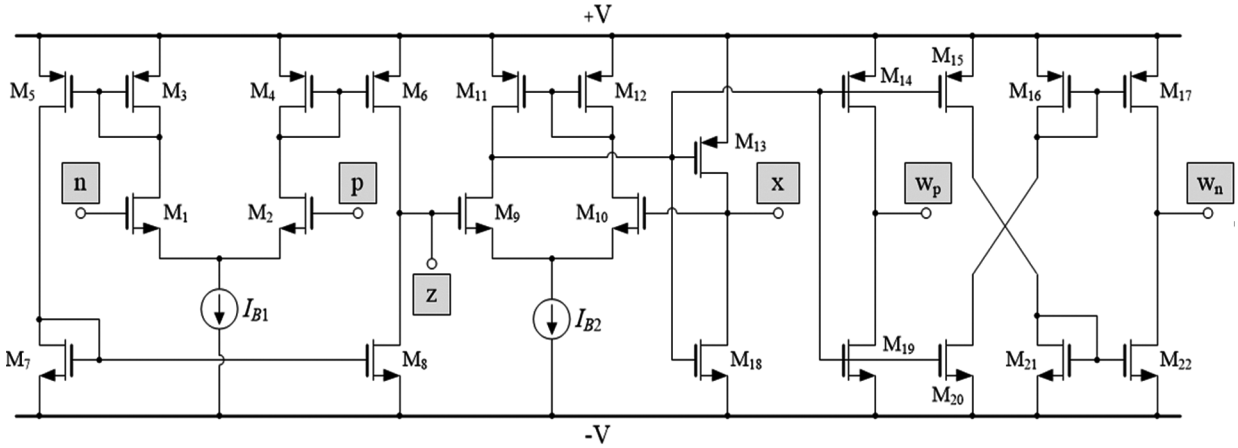

Fig. 2 — CMOS implementation of the VDCC

transistors M_1 and M_2, and I_{B1} is the external DC bias current. The proposed FDNR simulator employing VDCC has been shown in Fig. 3, which employs single VDCC along with two grounded capacitances (C_1 and C_2). Now, routine circuit analysis of Fig. 3 yields the following input impedance:

$$Z_{in} = \frac{v_{in}}{i_{in}} = \frac{g_m}{s^2 C_1 C_2} = \frac{1}{s^2 D_{eq}}, \quad \text{... (3)}$$

where the realized FDNR, D-element value is computed as;

$$D_{eq} = \frac{C_1 C_2}{g_m} \quad \text{... (4)}$$

It can be observed from Eq.(4) that the value of D_{eq} can be varied through g_m, which is controlled by the external biasing current I_B.

3 Non-ideal Analysis

3.1 Effect of frequency-dependent transconductance (g_m)

In this section, the effect of frequency dependent transconductance of VDCC block on the realized FDNR simulator has been investigated. In ideal condition, it has been assumed that transconductance of the VDCC is not a frequency dependent parameter, but in practical scenario the gm may be a function of frequency. Now, considering the single-pole frequency limited behavior of g_m it can be defined as g_m` as, $g'_m = \frac{g_{m0}}{1 + s\tau}$

Now, the input impedance Z_{in} from Eq. (3) can be modified as;

$$Z_{in} = \frac{g_{m0}}{s^2 C_1 C_2 (1 + s\tau)} \quad \text{... (5)}$$

On further simplifying,

$$Z_{in} = \frac{1}{\left(\frac{1}{g_{m0} / s^2 C_1 C_2}\right) + \left(\frac{1}{1/ s^3 \tau C_1 C_2}\right)} \quad \text{... (6)}$$

The equivalent network of Eq. (6) can be deduced as given in Fig. 4, in which the equivalent values of D'_{eq} and Z' can be given as:

$$D'_{eq} = \frac{C_1 C_2}{g_{m0}} \quad \text{... (7)}$$

and $Z' = \frac{1}{s^3 \tau C_1 C_2}$ ... (8)

3.2 Effect of non-ideal voltage/current transfer ratios

The current-voltage relations of VDCC ports, considering non-ideal current/voltage/transconductance gains can be described by the following equations.

$$\begin{bmatrix} i_p \\ i_n \\ i_z \\ v_x \\ i_{wp} \\ i_{wn} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ \alpha g_m & -\alpha g_m & 0 & 0 \\ 0 & 0 & \beta & 0 \\ 0 & 0 & 0 & \gamma_p \\ 0 & 0 & 0 & -\gamma_n \end{bmatrix} \cdot \begin{bmatrix} v_p \\ v_n \\ v_z \\ i_x \end{bmatrix}, \quad \text{... (9)}$$

where α, β and γ are the non-ideal transconductance, voltage, and current transfer ratios of the VDCC, respectively (ideally, their values are equal to unity).

The FDNR impedance taking Eq. (9) into account can be found as;

$$Z_{in} = \frac{v_{in}}{i_{in}} = \frac{\alpha\beta\gamma_p g_m}{s^2 C_1 C_2}, \quad \text{... (10)}$$

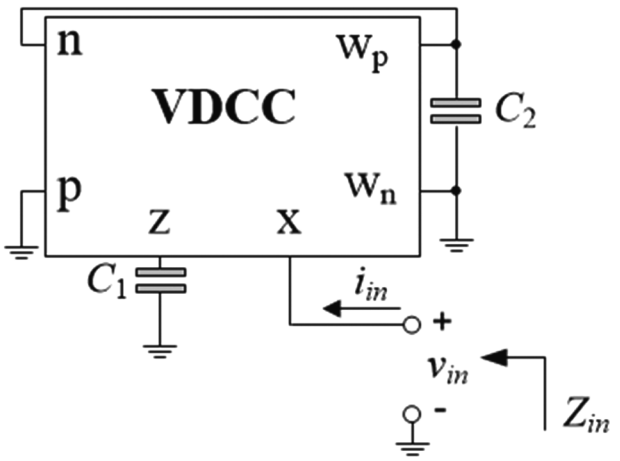

Fig 3 — Proposed FDNR simulator circuit

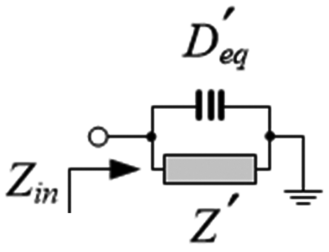

Fig. 4 — Equivalent network derived using Eq. (6).

where FDNR value can be computed as;

$$D_{eq(non-ideal)} = \frac{C_1 C_2}{\alpha\beta\gamma_p g_m} \quad \text{... (11)}$$

3.3 Effect of non-ideal gains with terminal parasitics

Furthermore, the parasitic model of VDCC is shown in Fig. 5, with different parasitic resistances and capacitances connected at the terminals in different configurations. This parasitic model was discussed in[45].

On replacing the ideal VDCC in the circuit shown in Fig. 3 with above VDCC parasitic model the modified impedance can be found out. For the input current i_{in}, using Eq. 9 the output current i_{wp} can be given as;

$$i_{wp} = -\gamma_p i_x = -\gamma_p i_{in}, \quad \text{... (12)}$$

where γ_p signifies the port ratio of the x and wp terminals. At w_p terminal the parasitic network is present as the shunt connection of R_n and C_n, and C_2 is also connected at the port, then using Eq. (9), the voltage at w_p port, v_{wp}, can be given as;

$$v_{wp} = -\gamma_p (R_n // C_n // C_2) i_{in} \quad \text{... (13)}$$

As per the circuit connection,

$$v_{wp} = v_n \quad \text{... (14)}$$

By further using Eq. (9) the port voltage of the Z terminal can be found as;

$$v_z = \alpha\gamma_p g_m (R_n // C_n // C_2)(R_z // C_1) i_{in} \quad \text{... (15)}$$

where R_z is the parasitic resistance present at the z port.

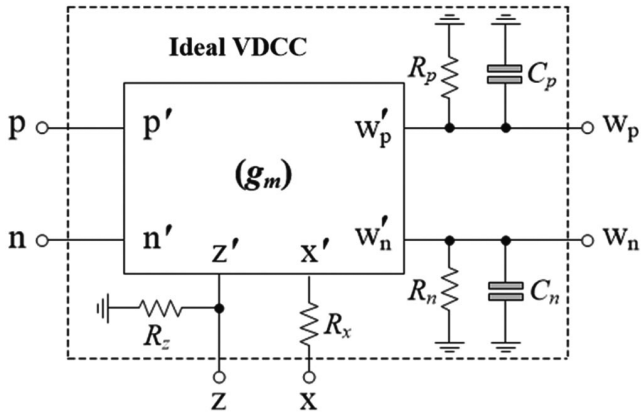

Fig. 5 — VDCC parasitic model given in [45]

The parasitic resistance R_x comes in the path of input current i_{in}, therefore,

$$v_x = v_{in} - i_{in} R_x \quad \text{... (16)}$$

By using the non-ideal matrix given in Eq. (9),

$$v_x = \beta v_z \quad \text{... (17)}$$

By using Eq.(15)-(17),

$$v_{in} = \left[\alpha\beta\gamma_p g_m (R_n // C_n // C_2)(R_z // C_1) + R_x\right] i_{in} \quad \text{... (18)}$$

Finally, the input impedance under the effect of non-ideal gains and port parasitics is found as;

$$Z_{in} = \frac{v_{in}}{i_{in}} = \alpha\beta\gamma_p g_m \left[\frac{1}{\frac{1}{1/s(C_n + C_2)} + \frac{1}{R_n}}\right]\left[\frac{1}{\frac{1}{1/sC_1} + \frac{1}{R_z}}\right] + R_x \quad \text{... (19)}$$

after further solving;

$$Z_{in} = \alpha\beta\gamma_p g_m \left[\frac{1}{s^2(C_n + C_2)C_1 + s\left(\frac{C_n + C_2}{R_z} + \frac{C_1}{R_n}\right) + \left(\frac{1}{R_z R_n}\right)}\right] + R_x \quad \text{... (20)}$$

From Eq.(20), we can deduce that the proposed FDNR circuit with consideration of port parasitics is always stable under any parameter of operating frequency related condition, as the coefficient of each term of the denominator is always positive in any condition. The equivalent network can be derived using Eq.(20) and it is shown in Fig. 6.

In Fig.6, the equivalent values of the components can be given as;

$$D'_{eq} = \frac{C_1(C_2 + C_n)}{\alpha\beta\gamma_p g_m} \quad \text{... (21)}$$

$$C' = \left(\frac{1}{\alpha\beta\gamma_p g_m}\right)\left[\frac{C_1}{R_n} + \frac{(C_2 + C_n)}{R_z}\right] \quad \text{... (22)}$$

$$R' = \alpha\beta\gamma_p g_m R_n R_z \quad \text{... (23)}$$

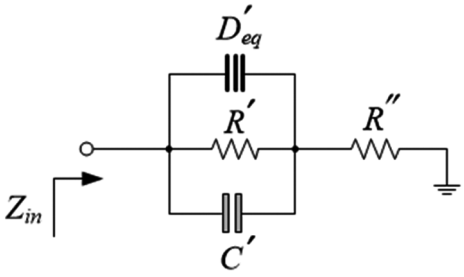

Fig. 6 — Equivalent network derived using Eq. (20).

and R'' is nothing but the resistance R_x connected at the x port.

3.4 Time domain analysis under the effects of port parasitic

In this analysis, we have tried to find out the nature of generated input current if a pure sinusoidal signal is applied across the parasitic equivalent network of Fig. 6. Suppose that the input voltage ($v_{in} = V_m \sin \omega t$) is applied across the network of Fig. 6. Practically, the R'' can be neglected at low and medium frequencies, and then input current can therefore be found out as;

$$i_{in} = I_m \sin(\omega t + \phi) \quad \text{... (24)}$$

where, from Eq.(24), the value of k and ϕ can be found as the following expressions, respectively;

$$I_m = \sqrt{\left[-\omega^2 C_1(C_2+C_n)+\frac{1}{R_n R_z}\right]^2 + \left\{\omega\left[\frac{C_1}{R_n}+\frac{(C_2+C_n)}{R_z}\right]\right\}^2} \quad \text{... (25)}$$

and

$$\phi = \tan^{-1}\left[-\frac{\dfrac{C_1}{R_n}+\dfrac{(C_2+C_n)}{R_z}}{\omega C_1(C_2+C_n)+\dfrac{1}{R_n R_z}}\right] \quad \text{... (26)}$$

For the phase to be 180°, as it is needed in the case of ideal FDNR, the condition will be;

$$\phi = \pi \quad \text{... (27)}$$

4 Simulation Results

To validate the theoretical analysis, SPICE simulations were performed employing CMOS VDCC[47]. The simulations have been performed with TSMC 0.18-μm CMOS process technology. The channel width to length ratios (W/L) of the employed NMOS and PMOS transistors were selected as shown in Table 2. The supply voltages and the bias current were chosen as: +V = -V = 0.75V and I_{B2} = 25 μA, respectively.

Fig. 7 shows the theoretical and simulated frequency responses of the proposed VDCC-based FDNR simulator in Fig. 3 with I_{B1} = 220 μA (g_m = 1 mA/V). The results are obtained for three different values of $C_1 = C_2$ (i.e., 20 pF, 50 pF and 100 pF), which result in D_{eq} = 0.4 aFs, 2.5 aFs, and 10 aFs, respectively. Both theoretical and simulated plots are shown in Fig.7. From impedance expression of the FDNR given in Eq.(3), it can be seen that as the frequency is increased the impedance realized by the proposed circuit decreases, which means impedance shows inverse frequency dependence. This behaviour can also be confirmed from Fig. 7.

Table 2 — Transistor dimensions of the CMOS VDCC in Fig.2

Transistor	W/L (μm/μm)
M_1-M_2, M_9-M_{10}	2.4/0.18
M_3-M_6, M_{11}-M_{13}, M_{15}-M_{17}	6/0.18
M_7-M_8, M_{19}-M_{22}	3/0.18
M_{14}, M_{18}	8/0.18

Furthermore, for the selected simulation parameters the total power consumption is found as 1.97 mW (with twenty-two transistors of VDCC) and the total power consumption is found as 1.28 mW (with 16 transistors neglecting M_{15}-M_{17} and M_{20}-M_{22} due to W_n terminal connected to ground).

Fig. 8 shows the magnitude-frequency responses of the proposed FDNR for various I_{B1} values. The plots depict the tunable nature of the realized FDNR controllable through biasing current I_{B1}. In Table 3, we have shown the component variation at the three different values of biasing current I_{B1}.

5 Applications of Grounded VDCC-Based FDNR

To show the workability of the designed synthetic FDNR, some application examples have been discussed. According to the concept proposed in[48], a passive RLC network can be transformed into a CDR network without changing the transfer function.

5.1. Second order Butterworth Low-pass and Band-stop filter realizations

The conventional second-order voltage-mode RLC low-pass filter (VMRLCLPF) and band-stop (VMRLCBS) filter have been shown in Fig. 9.

The transfer functions of the second-order VMRLCLPF and VMRLCBS shown in Fig. 9 are given by Eqs. (28) and (29), respectively.

$$\frac{v_{out}}{v_{in}} = \frac{1}{s^2 L_{LP} C_{LP} + s R_{LP} L_{LP} + 1} \quad \text{... (28)}$$

$$\text{and } \frac{v_{out}}{v_{in}} = \frac{s^2 C_{BS} L_{BS} + 1}{s^2 L_{BS} C_{BS} + s R_{BS} C_{BS} + 1} \quad \text{... (29)}$$

It is evident from the above transfer functions, the denominators in both filters are the same, from which the natural angular frequency (f_o) and the quality factor (Q) for $R = R_{LP} = R_{BS}$, $L = L_{LP} = L_{BS}$ and $C = C_{LP} = C_{BS}$ are obtained as follows:

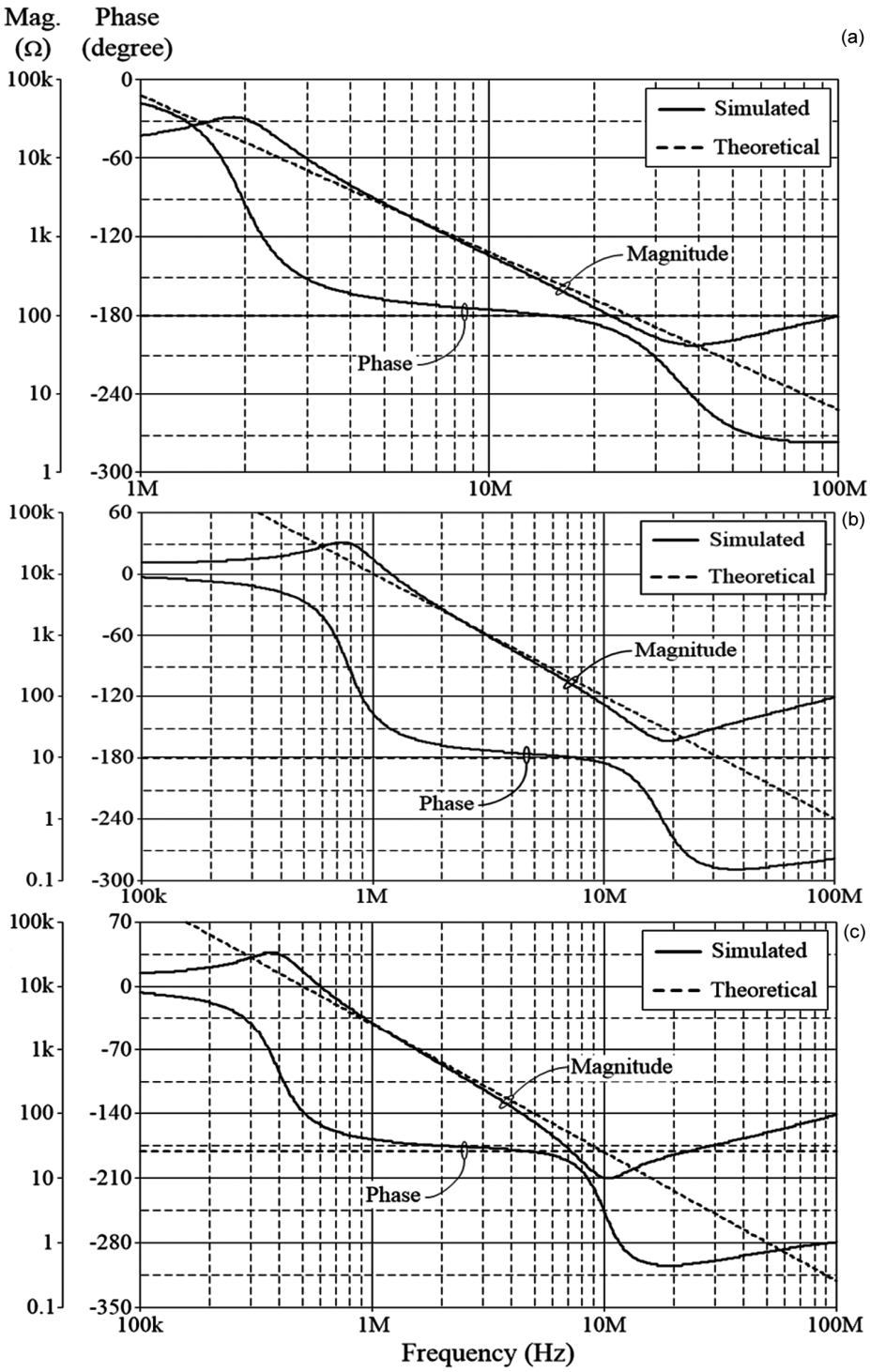

Fig. 7 — Theoretical and simulated frequency responses of the proposed VDCC-based FDNR simulator in Fig. 3. (a) $C_1 = C_2 = 20$ pF (b) $C_1 = C_2 = 50$ pF (c) $C_1 = C_2 = 100$ pF

$$f_o = \frac{\omega_o}{2\pi} = \frac{1}{\sqrt{LC}} \quad \text{... (30)}$$

and $$Q = \frac{1}{R}\sqrt{\frac{L}{C}} \quad \text{... (31)}$$

Interestingly, Eqs. (30) and (31) show that the Q-value can be tuned independently by changing the value of R for which the f_o-value remains unchanged. The component values of the above prototypes and their corresponding parameters f_o and Q for three

different values of R are given in Table 4. Applying the scaling magnitude $k_m = 10^9$, the component values given in Table 4 are obtained as given in Table 5. Now on applying the Bruton's transformation technique the RLC filters shown in Fig. 9 (VMRLCLPF and VMRLCBSF) can be transformed to their CDR counterparts (VMCDRLPF and VMCDRBSF) as depicted in Fig. 10.

Now, the transfer functions of VMCDRLPF and VMCDRBSF have been given by Eq. 32 and 33;

$$\frac{v_{out}}{v_{in}} = \frac{1}{s^2 R_{tf} C_{tf} D_{eq} + s D_{eq} + C_{tf}} \quad \text{... (32)}$$

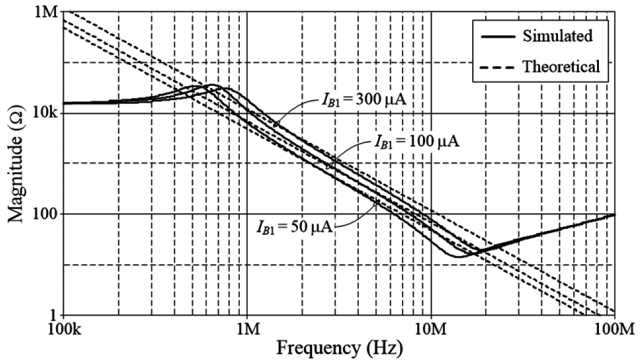

Fig 8 — Magnitude-frequency responses of the proposed FDNR for various I_{B1} values.

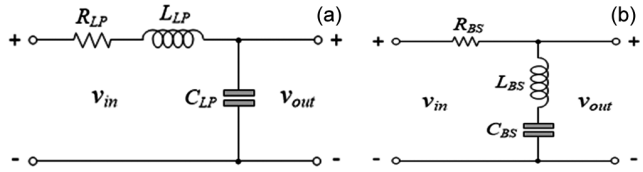

Fig 9 — Passive RLC second-order filter prototypes (a) LP filter (b) BS filter

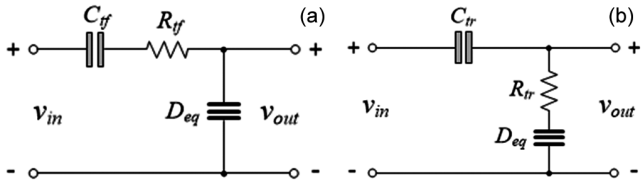

Fig 10 — Transformed CRD filters. (a) second-order LP filter (b) second-order BS filter

and $$\frac{v_{out}}{v_{in}} = \frac{s^2 R_{tf} C_{tf} D_{eq} + C_{tf}}{s^2 R_{tf} C_{tf} D_{eq} + s D_{eq} + C_{tf}} \quad \text{... (33)}$$

The transformed element values for three different values of D_{eq} are given in Table 6.

As a consequence, the D-element can be emulated by the proposed VDCC-based FDNR in Fig. 3 with the components given in Table 7.

The ideal and simulated frequency responses of the transformed CRD LP and BS filters in Fig.10 (a) & 10(b) for cases I, II, and III are shown in Figs. 11 & 12, respectively.

5.2. Third-Order Butterworth LP Filter Realization

Now, the doubly-terminated RLC ladder filter network to generate normalized third-order

Table 3 — Variation of the FDNR value due to change in biasing current I_{B1} at $C_1 = C_2 = 50$ pF and difference between theoretical and simulation values

I_{B1} (μA)	g_m (mA/V)	D_{eq} (aFs)	Z_{in} (kΩ)		Error (%)
			Simulation	Theory	
50	0.43	5.24	1.23	1.19	2.85
100	0.67	3.70	1.90	1.69	12.48
300	1.17	2.14	2.77	2.92	5.19

Table 4 — Component values of Fig. 9 and their parameters f_o and Q for three different values of R.

Case	R (kΩ)	L (mH)	C (nF)	f_o (Hz)	Q
I	0.68	2.2	4.7	50	1
II	1.5	2.2	1	107.3	1
III	2.7	2.2	0.33	186.79	1

Table 5 — Denormalized component values of Fig.9 with $k_m = 10$

Case	R_{new} (GΩ)	L_{new} (mH)	C_{new} (fF)
I	0.68	2.2	4.7
II	1.5	2.2	1
III	2.7	2.2	0.33

Table 6 — Transformed element values

Case	R_{tf} (kΩ)	C_{tf} (nF)	D_{eq} (fFs)
I	2.2	1.47	4.7
II	2.2	0.68	1
III	2.2	0.37	0.33

Table 7 — Component values of Fig.10 and corresponding f_o for three different values of D_{eq}.

Case	D_{eq} (fFs)	I_B (μA)	g_m (mA/V)	$C_1 = C_2$ (nF)	f_o (kHz)		Error in f_o (%)
					Theoretical	Simulation	
I	4.7	50	0.48	1.5	50	52	5.07
II	1	220	1	1.0	107.30	109.40	1.96
III	0.33	125	0.75	0.5	186.79	199.53	6.82

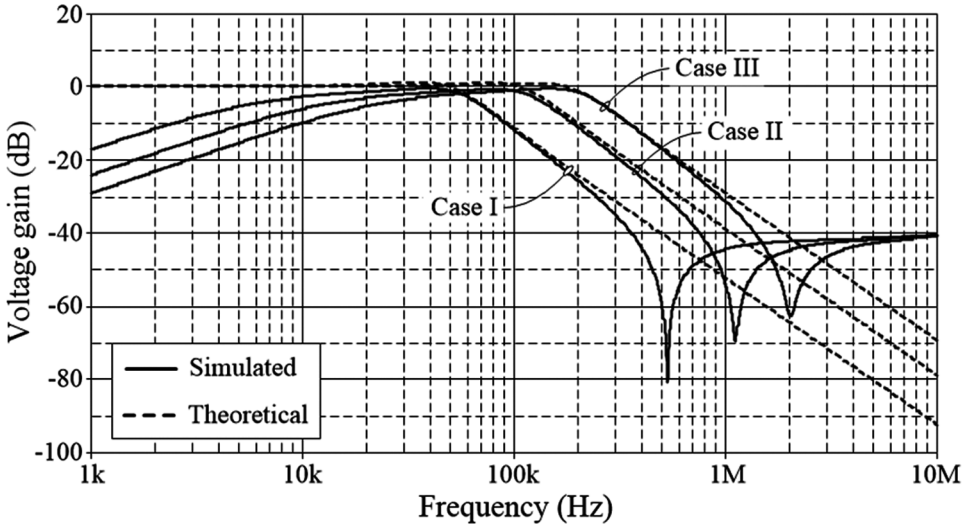

Fig 11 — Ideal and simulated frequency responses of the transformed CRD LP filter in Fig. 10(a).

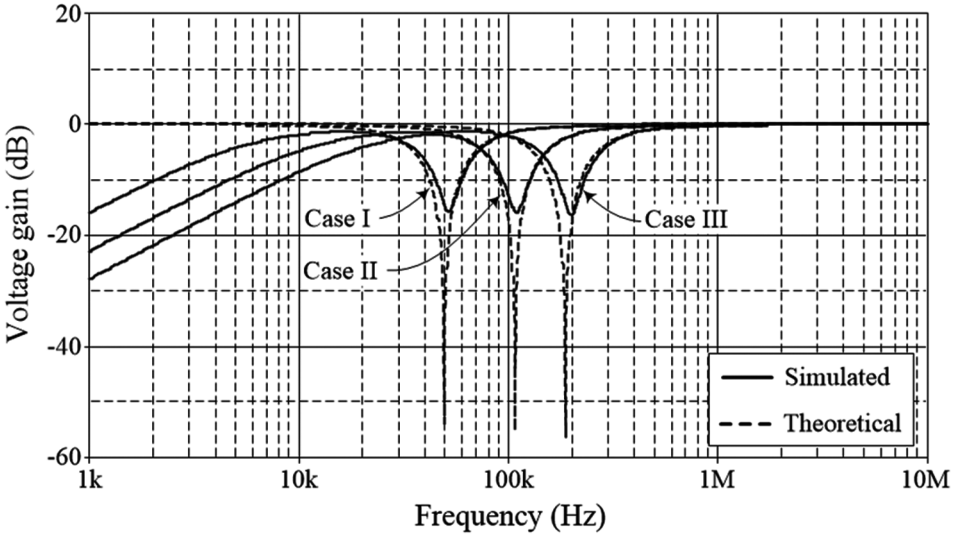

Fig 12 — Ideal and simulated frequency responses of the transformed CRD BS filter in Fig. 10(b)

Butterworth LP response is shown in Fig. 13, where $R_S = R_L = 1$ Ω, $L_1 = L_3 = 1$ H, and $C_2 = 2$ F. After applying the scaling technique with scaling magnitude $k_m = 10^9$ and scaling frequency $k_f = 628$ krad/s, the passive components of Fig. 13 are changed to; $R_S = R_L = 1$ GΩ, $L_1 = L_3 = 1.59$ kH, and $C_2 = 3.18$ fF.

Using Bruton's transformation, the RLC passive ladder filter of Fig.13 is transformed to Fig. 14 and the corresponding components are obtained as; $C_S = C_L = 1$ nF, $R_1 = R_3 = 1.59$ kΩ, and $D_2 = 3.18$ fFs.

To simulate $D_2 = 3.18$ fFs, the proposed VDCC-based FDNR simulator circuit of Fig.3 is realized with the following components; $I_B = 110$ μA ($g_m = 0.71$ mA/V) and $C_1 = C_2 = 1.5$ nF. Now, Fig. 15 shows the ideal and simulated frequency responses of the transformed 3rd-order Butterworth LP filter given in Fig. 14.

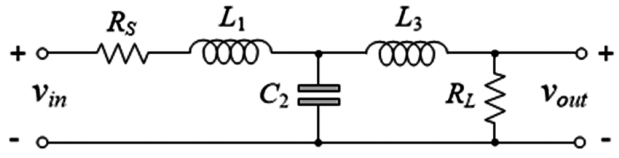

Fig 13 — Third-order Butterworth LP ladder filter.

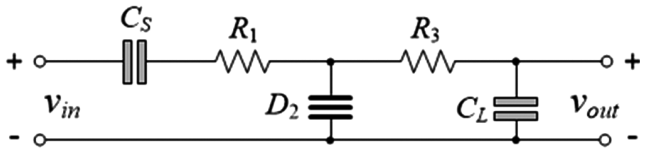

Fig 14 — Transformed 3rd-order Butterworth CRD LP filter.

6 Experimental Verification of the Proposed FDNR Simulator

Now, the performance of the proposed FDNR simulation circuit has been experimentally verified through the prototype developed using commercially available integrated circuits (ICs), IC CA3080 and IC AD844. The CA3080 is a current-controlled IC for a single current-output transconductance amplifier, while the AD844 IC replicates the function of the second-generation current conveyor. The CA3080 and AD844 based implementation of VDCC has been shown in Fig.16. Furthermore, as suggested by the manufacturer, the transconductance (g_m) of IC CA3080 linearly depends on the external DC bias current I_B ($g_m = 20I_B$ [49]). In Fig.17, the physical implementation of the VDCC (employed in the FDNR simulator) has been shown, which is based on the CA3080 and AD844 ICs. To obtain the experimental results, the supply voltages were taken as ±5V.

The Figs.18-21 represent the experimentally measured frequency response characteristics for the input impedance (Z_{in}) of the proposed VDCC-based

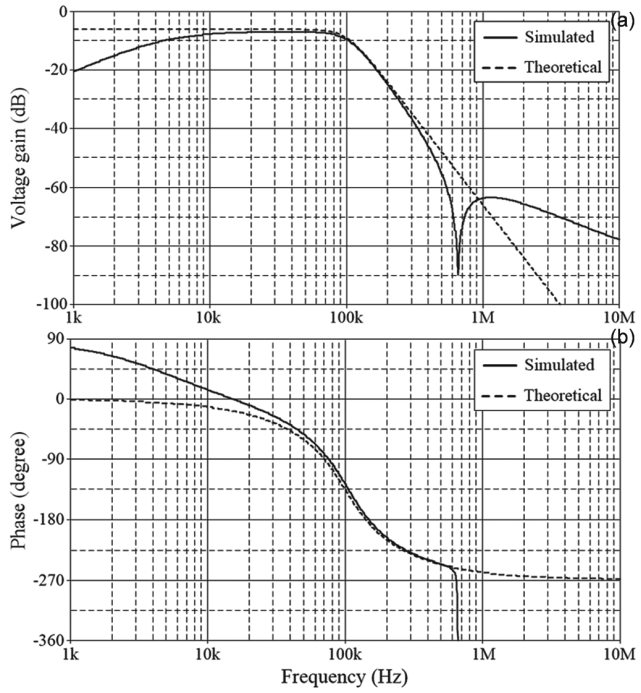

Fig 15 — Ideal and simulated frequency responses of 3rd-order Butterworth LP ladder filter in Fig. 14

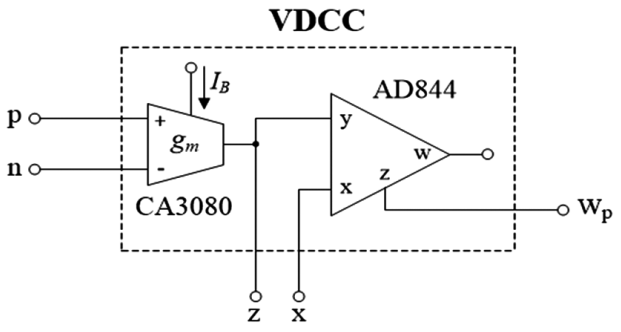

Fig. 16 — Internal implementation of VDTA; the single output OTAs can be realized by CA3080

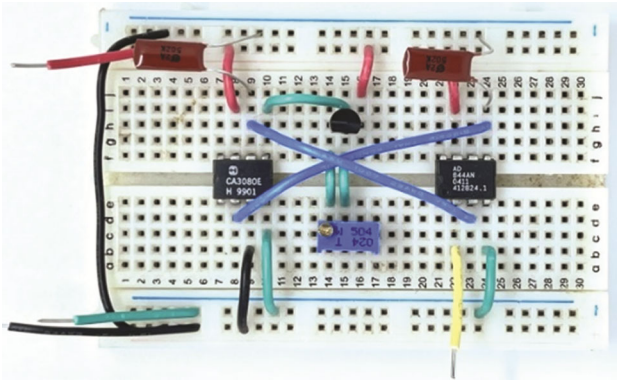

Fig. 17 — Experimental setup based on CA3080 and AD844 to implement employed VDCC

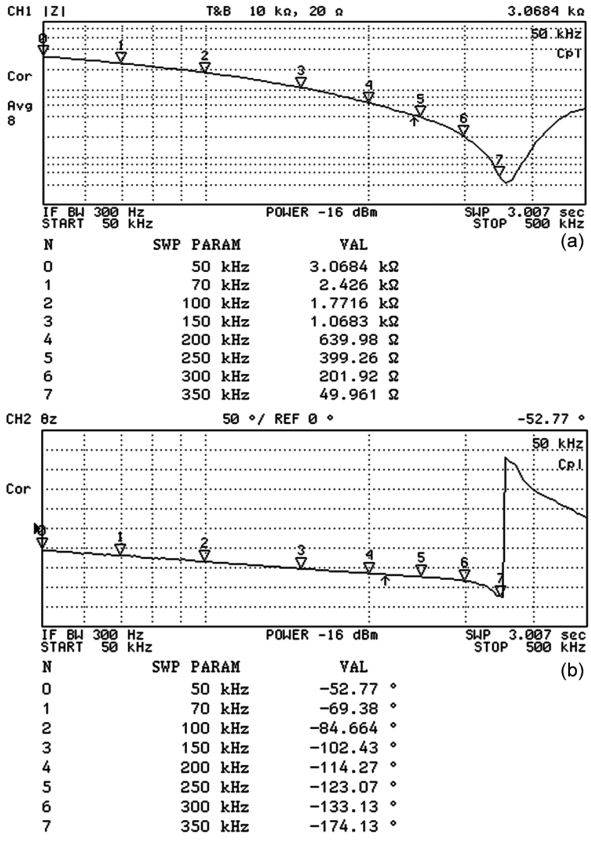

Fig. 18 — Measured frequency characteristics for Z_{in} of the proposed VDCC-based FDNR simulator in Fig.3 with g_m = 0.25 mA/V (I_B = 12.5 μA). (a) magnitude-frequency response (b) phase-frequency response

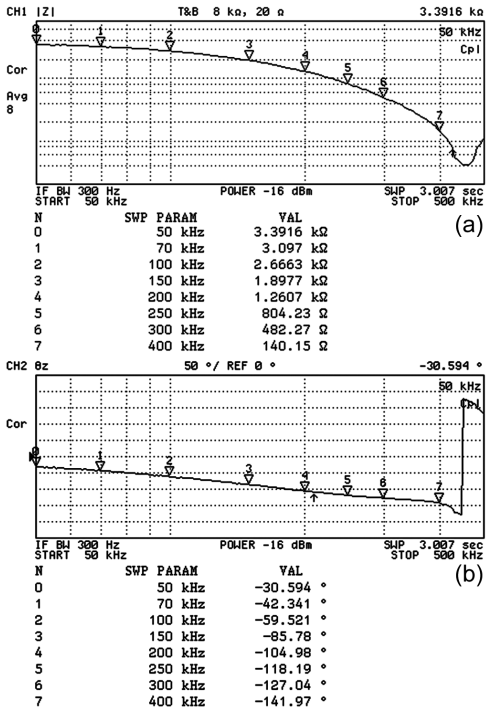

Fig. 19 — Measured frequency characteristics for Z_{in} of the proposed VDCC-based FDNR simulator in Fig.3 with g_m = 0.5 mA/V (I_B = 25 μA). (a) magnitude-frequency response (b) phase-frequency response

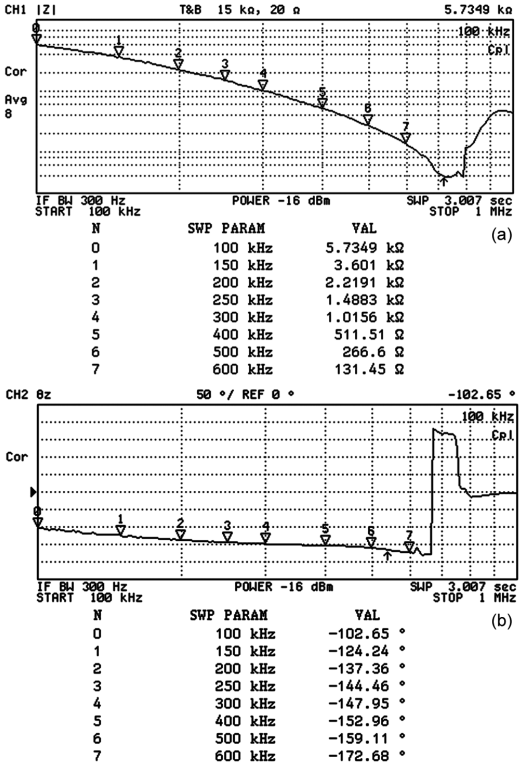

Fig. 20 — Measured frequency characteristics for Z_{in} of the proposed VDCC-based FDNR simulator in Fig.3 with g_m = 1 mA/V (I_B = 50 μA). (a) magnitude-frequency response (b) phase-frequency response

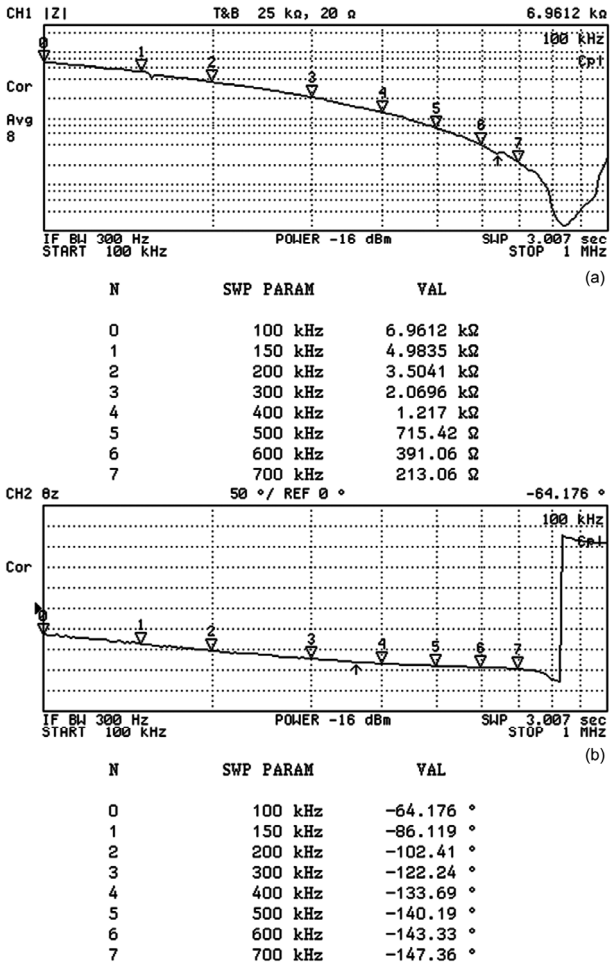

Fig. 21 — Measured frequency characteristics for Z_{in} of the proposed VDCC-based FDNR simulator in Fig.3 with g_m = 2 mA/V (I_B = 100 μA). (a) magnitude-frequency response (b) phase-frequency response

FDNR simulator in Fig. 3 with $C_1 = C_2 = 0.5$ nF. The measured results are obtained for g_m = 0.25 mA/V, 0.50 mA/V, 1 mA/V, and 2 mA/V (I_B = 12.5 μA, 25 μA, 50 μA, and 100 μA), resulting in D_{eq} = 1 fFs, 0.5 fFs, 0.25 fFs, and 0.125 fFs, respectively.

7 Conclusion

This work reports a highly compact resistor-less circuit architecture (based on only single VDCC and two grounded capacitances) for FDNR simulator with the facility of electronic tuning. The presented FDNR simulator realizes a loss-less FDNR function without following any parameter/components related condition(s). The behavior of proposed circuit has been investigated considering the frequency dependence transconductance gain, non-ideal current-voltage tracking errors, and terminal parasitics of

employed VDCC. From the parasitic analysis it can be observed that reported circuit enjoys stable operation for any range of operating/circuit parameters. The working of realized FDNR simulator has been validated by higher-order filtering circuit examples. The performance of the developed circuits has been verified by SPICE simulations with TSMC CMOS technology for 0.18µm. The experimental verification of the developed VDCC based synthetic FDNR has been discussed by using commercially available ICs CA3080 and AD844.

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