Indian Journal of Pure & Applied Physics
Vol. 60, October 2022, pp. 855-865
DOI: 10.56042/ijpap.v60i10.63908

Cost-effective Programmable Logic Arrays Using Multilayer Structures of Decoders in QCA Framework

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Received 18 June 2022; accepted 16 September 2022

The emerging nanotechnology paradigm, Quantum Dot Cellular Automata (QCA) in particular, is gaining a wide recognition due to its high speed, nano feature size and considerably low power consumption. The QCA architecture not only provide potential alternative for Complementary Metal Oxide Semiconductor (CMOS) circuits but its multilayer topology facilitates an added benefit of cost efficacy and immunity towards random interference. Moreover, design of programmable logic devices in QCA is vital to promote the multi-utility and resiliency of the computing circuits. This paper presents the multilayer designs of 2×4 and 3×8 decoder circuits in QCA framework with 55.1% and 51.17% better cost efficiency respectively, over the earlier reported designs. The presented 3×8 decoder circuit is further utilized to implement Programmable Logic Array (PLA) to realize Boolean functions of adder and subtractor. The presented circuits are cost effective and showcase the significance of programmable devices in nano-computing.

Keywords: QCA; PLA; Decoder; Adder; Subtractor

1 Introduction

The continuous demand of portable, ultra low power and high speed devices is gathering attention from scientific community towards the nanotechnology paradigms. The physical and technological constraints of CMOS technology such as power consumption, leakage currents and interconnects dominance at nano-scale are leading to the evolution of newer technologies that may potentially substitute the CMOS in near future[1]. QCA is one of such technologies that have capability to adhere to the demands of size, power and speed in electronic industry. The power dissipation is extremely low in QCA as it doesn't work with flow of current or voltage, rather it works with the change in cell polarization[2]. QCA circuit is likely to operate with high frequency clock of the order of terahertz[3] and with high packaging density[4]. The experimental demonstration of QCA devices was verified in the past[5,6]. The major limitation of QCA about its operability was also overcome by introducing its room temperature operation in[7]. The fabrication of quantum dots in various categories such as metal dots[2] and GaAs/AlGaAs doped hetero-structures[8] peratingat cryogenic temperatures while silicon dangling bonds[9] and molecular dots[10] operating at room temperature were established in the past.

The fundamental unit of QCA is a QCA cell with four quantum dots at four corners of the cell. Two diagonal dots are occupied with the electrons resulting in two steady states of polarization forming logic 1 and logic 0 binary states as shown in Fig. 1(a). Due to Coulombic interaction, the polarization of adjacent cells becomes identical resulting in the QCA wire carrying information (Fig. 1(b). Majority voter and inverter form the preliminary components[11] in QCA architectures as shown in Fig. 1(c & d). The directed information flow from one end to other in QCA circuit is achieved using an adiabatic clock with four phases (Fig. 1(f)). The adiabatic clock in QCA has four zones (Fig. 1(e)) and each zone carries clock signal phase shifted by 90°. The latency in the QCA circuit is obtained by estimating number of clock zones lying on the shortest path between input and output.

Most of the QCA architectures designed so far in the literature are coplanar. In QCA circuits, the use of crossovers is inevitable. If the crossovers are coplanar, they are prone to random interference while multilayer crossovers are immune to the crosstalk[12]. Moreover, multilayer wire crossing produces lesser delay in comparison with its coplanar counterpart[13]. In

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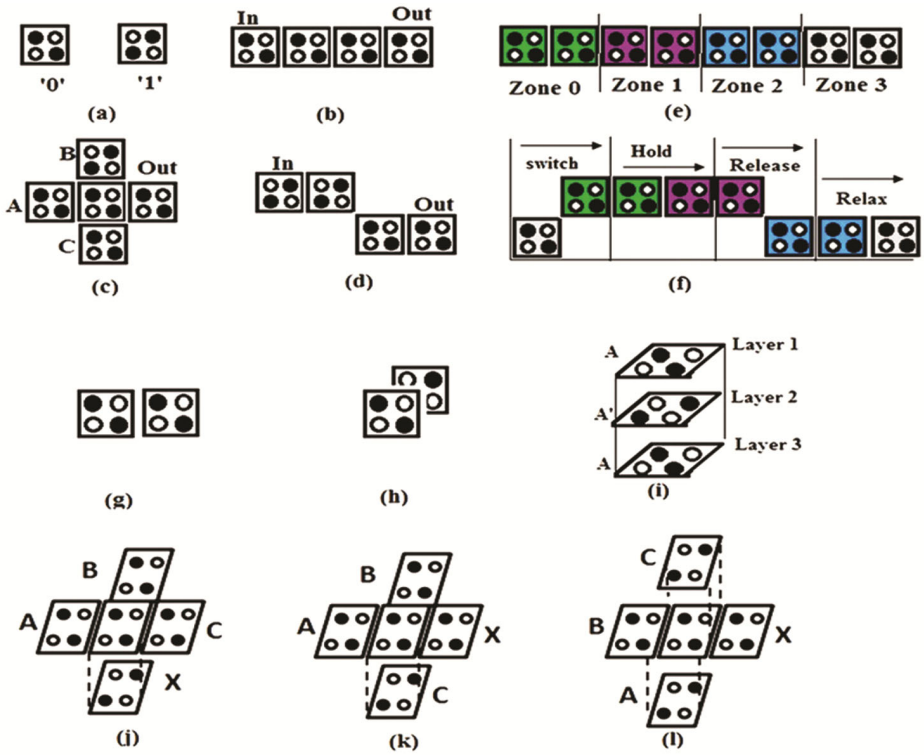

Fig. 1 — (a) QCA cells with binary states (b) QCA wire (c) Majority voter (d) Inverter (e) Clock zones (f) Clock phases (g) edge-wise aligned cells (h) facing cells (i) cells on three layers (j) M(x) = (AB1+ BC1+AC)' (k) M(x) = (AB+BC'+AC') (l) M(x) = (A'B+BC+A'C).

addition to this, it is noteworthy, that in multilayer QCA structures, the active components can be placed on the different layers unlike CMOS[14] and thus, the multilayer architectures become more cost efficient in QCA framework over the coplanar one. Gin *et al.* has presented the feasible QCA architectures in multilayer topology[14] and reported the alternative geometry of majority gates as shown in Fig. 1. The QCA cells that are edge-wise aligned have same polarization but, the cells facing each other have opposite polarization as portrayed in Fig. 1(g&h) respectively. The polarization states of three layer QCA cells are shown in Fig. 1(i). Thus, the placement of QCA cells in multilayer QCA design is carried out by considering the fact that each layer receives inverted logic from its previous layer. The possible designs and equations for multilayer majority voters are shown in Fig. 1 (j, k, l). Although, the fabrication of multilayer QCA structures is difficult, the inherent advantages of multilayer QCA designs such as stability, efficacy, reduced delay and immunity towards external arbitrary disturbances motivate researchers to give their viewpoint on multilayer QCA designs.

Several papers have been presented on QCA coplanar designs but their multilayer structures are not much addressed. Sen *et al.* reported the design of adder, multiplexer and some sequential latches in[15-17]. The multilayer design of arithmetic logic unit has been reported in[18]. Moreover, some other multilayer circuits including configurable logic block[19], shift registers[20] and RAM cell[21] have been presented in the literature. The design of configurable or programmable logic structure is not much discussed in the existing literature. This paper presents the multilayer designs of 2×4 and 3×8 decoders for the application of programmable logic array (PLA). The major contributions of this paper are as follows:

- Design of cost efficient multilayer 2×4 decoder with QCA analysis.
- Design and analysis of cost effective3×8 decoder which is further employed to obtain the structure of PLA.
- Design of generic PLA to configure adder and subtractor functions.

This paper is organized in five sections. Introduction and related are presented in section I and II respectively. Section III depicts proposed QCA design architectures for multilayer decoders. Section IV presents the methodology and PLA design for the

application of adder and subtractor. The comparative study with results and discussion is proposed in section V. Section VI gives conclusion.

2 Related works

Decoder being the most crucial component in digital logic design area has been addressed by many researchers in the past. Kianpour *et al.* proposed the coplanar 2×4 decoder with 270 cells and 3×8 decoder with 1074 QCA cells[22]. In the series of development, many researchers optimize the design of decoder in terms of cell count, area and latency[23-26]. The main aim while dealing with QCA circuits is to optimize performance parameters such as number of cells, delay, number of majority voters and finally cost function. De *et al.* has developed coplanar 2×4 and 3×8 decoders using multilayer crossovers with 93 and 270 cells[27].This paper presents the XOR based designs of decoders and also includes the design of 4×16 decoder and its PLA implementation. Later, attempt has been made to realize decoders using matrix representation method[25]. Also, in another attempt QCA ROM design has been reported with 4-bit row/column decoder by Mukherjee *et al.* in[28].

3 Proposed QCA design architectures

This section presents the design of cost efficient 2x4 and 3x8 decoders using multilayer approach. These decoders serve as basic modules for the design of PLA. Multilayer topology produces the area efficient circuits.

3.1 Multilayer QCA design of 2x4 decoder

The 2x4 decoder circuit is implemented here using majority gates and inverters as shown in Fig. 2. It has two inputs A , B and four outputs

$X_1 = \overline{A}\overline{B}$, $X_2 = \overline{A}B$, $X_3 = A\overline{B}$, $X_4 = AB$

The novel QCA implementation of this 2x4 decoder using multilayer topology is shown in Fig. 3.

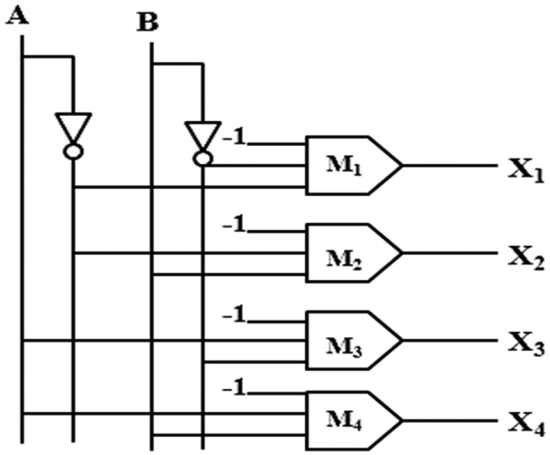

Fig. 2 — Schematic for 2x4 decoder.

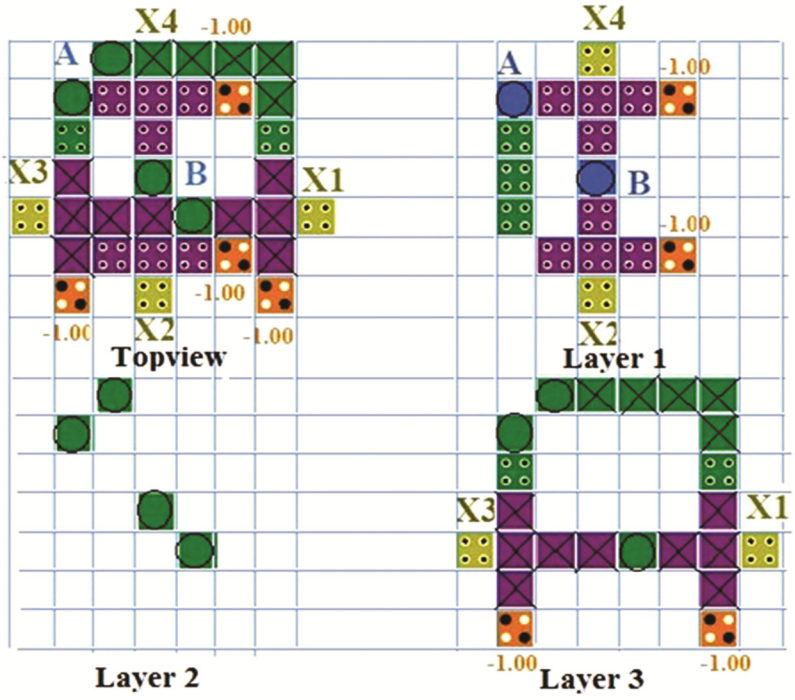

Fig. 3 — Three layer structure of 2x4 decoder depicting top-view, layer 1, layer 2 and layer 3.

The implementation shows three-layer structure of proposed decoder circuit with two majority gates $M_2(\overline{A}, B, 0)$ and $M_4(A, B, 0)$ on layer 1 producing outputs X_2 and X_4. Layer 2 holds via or interconnects and layer 3 has remaining majority gates $M_1(\overline{A}, \overline{B}, 0)$ and $M_3(A, \overline{B}, 0)$ producing output X_1 and X_3. The latency of the circuit is 0.5 clock (2 clock zones). The proposed three layer decoder is novel and compact with minimum delay. The QCA structures are designed and simulated on QCA Designer 2.0.3 tool[29]. Here, each QCA cell has 18nm x 18nm dimensions with 2nm spacing between the cells. In the multilayer structures, each layer is separated from the other layer by the distance of 11.5nm for getting the error free operation. The simulation waveform for the proposed 2x4 decoder is shown in Fig. 4.

3.2 Multilayer QCA design of 3x8 decoder

The design of 3x8 decoder in QCA framework is presented in this section with the multilayer approach. This circuit has three inputs A, B, C and eight outputs Y_0, Y_2, Y_7 as shown in Fig. 5. The QCA implementation is carried out in three layers to optimize the performance parameters. The same module of 2x4 decoder is extended to form 3x8 decoder. In Fig. 5, 3x8 decoder is implemented using total twelve majority voters with six majority gates on layer 1while remaining six majority voters on layer 3. Layer 2 carries the interconnects between layer 1 and layer 3. Latency of the proposed circuit is 1 clock cycle (4 clock zones).

The equations realizing output functions of decoder using majority gates are depicted in Eq. 1 to Eq.8. Correctness of the circuit can be validated from the simulation waveform of the proposed QCA design of 3x8 decoder as depicted in Fig. 6. Each output of decoder becomes logic 1when corresponding data appears on its input bus. For example, when input bus ABC = 000, the output Y_0 becomes logic 1.

$$Y_0 = M_1(X_1, C, 0) = M_1(M(\overline{A}, \overline{B}, 0), C, 0)) \quad \ldots (1)$$

$$Y_1 = M_2(X_1, \overline{C}, 0) = M_2(M(\overline{A}, \overline{B}, 0), \overline{C}, 0)) \quad \ldots (2)$$

$$Y_2 = M_3(X_2, C, 0) = M_3(M(\overline{A}, B, 0), C, 0)) \quad \ldots (3)$$

$$Y_3 = M_4(X_2, \overline{C}, 0) = M_4(M(\overline{A}, B, 0), \overline{C}, 0)) \quad \ldots (4)$$

$$Y_4 = M_5(X_3, C, 0) = M_5(M(A, \overline{B}, 0), C, 0)) \quad \ldots (5)$$

$$Y_5 = M_6(X_3, \overline{C}, 0) = M_6(M(A, \overline{B}, 0), \overline{C}, 0)) \quad \ldots (6)$$

$$Y_6 = M_7(X_4, C, 0) = M_7(M(A, B, 0), C, 0)) \quad \ldots (7)$$

$$Y_7 = M_8(X_4, \overline{C}, 0) = M_8(M(A, B, 0), \overline{C}, 0)) \quad \ldots (8)$$

4 Methodology and PLA design

This section describes the methodology, design and QCA implementation of Programmable Logic Array with its application as adder and subtractor.

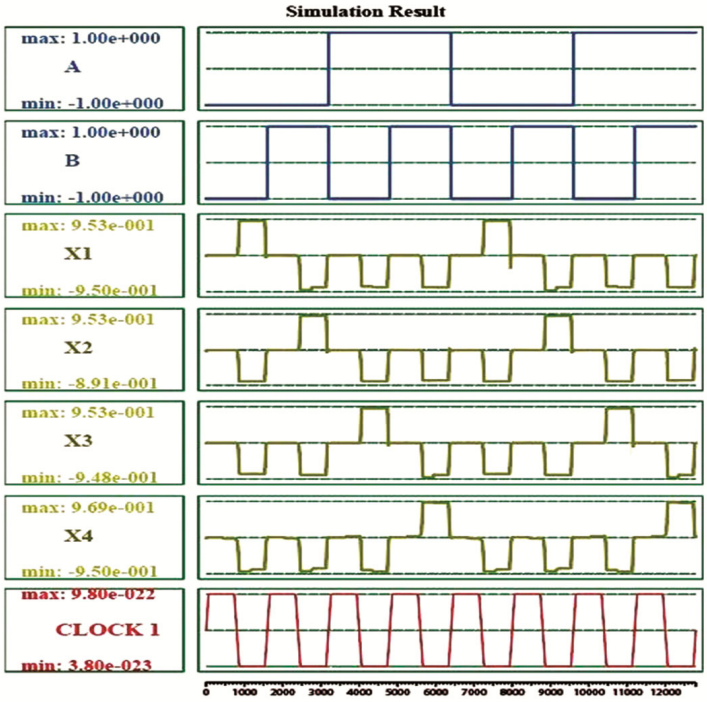

Fig. 4 — Simulation waveform of proposed three layer QCA 2x4 decoder.

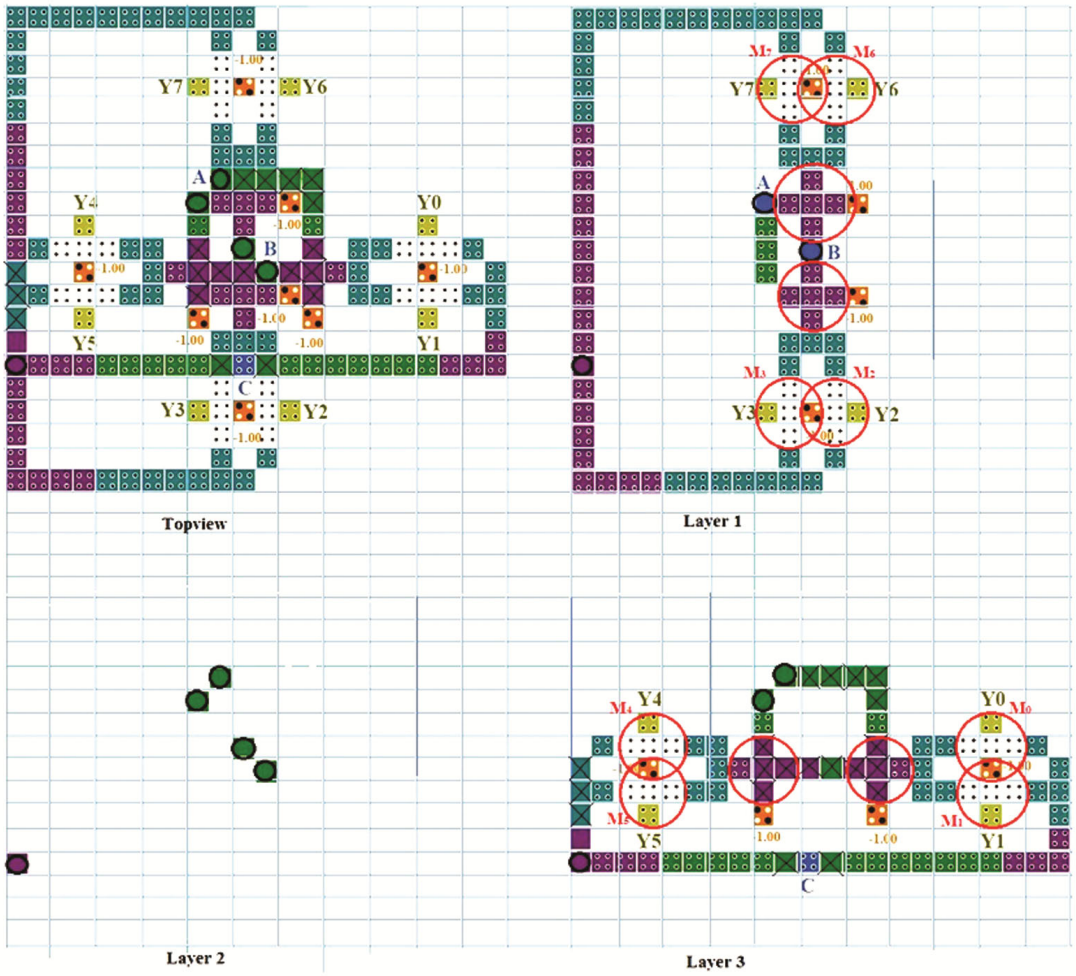

Fig. 5 — Three layer QCA structure of proposed 3x8 decoder depicting top-view, layer1, layer 2 and layer 3.

4.1 Methodology

The design of decoder can be initiated from 1:2 decoder and can be extended upto n:2^ndecoder using a suitable algorithm. This decoder design can be further extended to design PLA circuit. The algorithm for the design of n x 2^n decoder from 1x 2 decoder is shown here. N[i] represents the variable names or inputs to the decoder. M gives the maximum number of input variables. K is the array of produced min-terms after obtaining the product. P is the length of k. Decoder circuit produces possible min-terms and the desired min-terms are summed up to produce sum-terms. The desired sum-term can generate the needed functions in PLA.

Algorithm

Design of PLA (N[i]-Variable Names, M- Max Number of variables, K: array representing minterms for the desired function, P=number of minterms in array K or length of K)

1. BEGIN
2. Input M
3. i=1
4. Input variable N[i]
5. Complement variable N[i] using NOT gate
6. MINTERMS = variable, variable complement
7. i=2

a. If i>M go to 9
b. Input variable N[i]
c. Complement variable N[i]using NOT gate
d. Make product terms using AND Gate with the existing MINTERMS using the variable N[i] and its complement
e. i=i+1

8. End of loop
9. j=1
10. From MINTERMS select K[j]
11. SUMTERM=K[j]

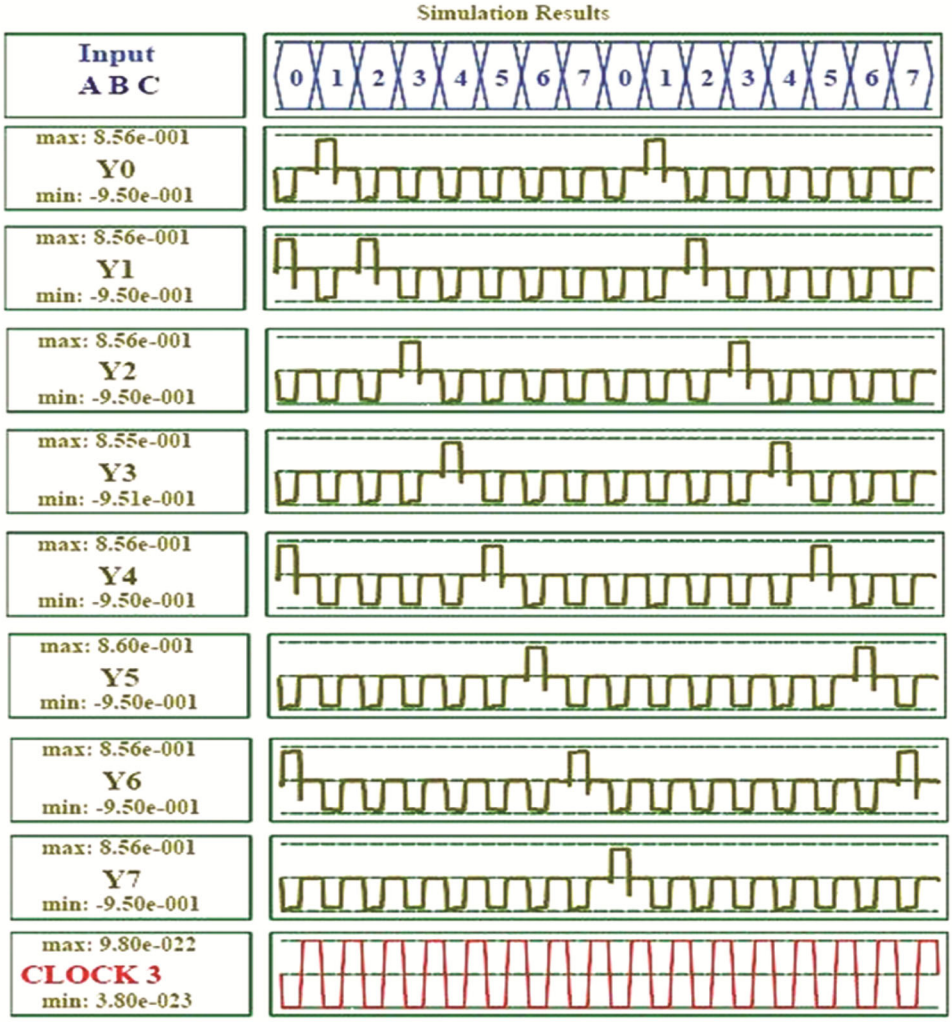

Fig. 6 — Simulation waveform for proposed three layer 3x8 decoder.

12. j=2
a. If j>P go to 13
b. From MINTERMS select K[j]
c. SUMTERM = compute sum of SUMTERM and K[j] using OR Gate
d. j=j+1
13. END
END

4.2 PLA design

The proposed algorithm can be experimentally implemented and fabricated using QCA. The product terms or min-terms are produced by 3x 8 decoder as Y_0, Y_1 to Y_7. The sum of these min-terms is then carried out using OR gate array. The PLA design to realize adder function is shown in Fig. 7. The sum terms for adder function are given by Eq. 9 and 10. The circuit is then realized using QCA as shown in Fig. 8 and its operation is validated from the simulation wave form as depicted in Fig. 9.

$$\text{Sum} = Y_1 + Y_2 + Y_4 + Y_7$$
$$\text{Sum} = \sum \text{m1, m2, m4, m7} \quad (9)$$
$$\text{Carry} = Y_3 + Y_5 + Y_6 + Y_7$$
$$\text{Carry} = \sum \text{m3, m5, m6, m7} \quad \ldots (10)$$

The QCA architecture of PLA, implementing adder function requires 12 majority gates (marked by red circles in Fig. 8) to realize product terms or min-terms and 6 majority gates (marked by green circles) to realize sum terms. The Sum terms $S_1 = Y_4 + Y_7$ and $S_2 = Y_1 + Y_2$ are obtained using two input OR gates. The final output function is generated as Sum = S_1 + S_2. Moreover, the final output function Carry = C_1 + C_2 where $C_1 = Y_3 + Y_5$ and $C_2 = Y_6 + Y_7$. Top-view of the circuit displays the merged view of all the layers.

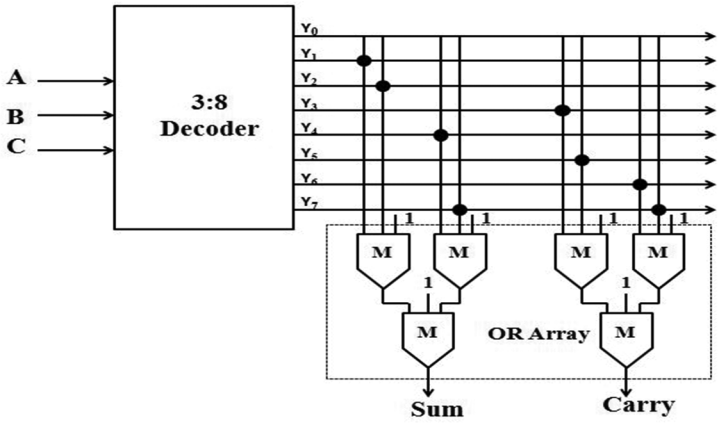

Fig. 7 — Schematic design of PLA using 3x8 decoder.

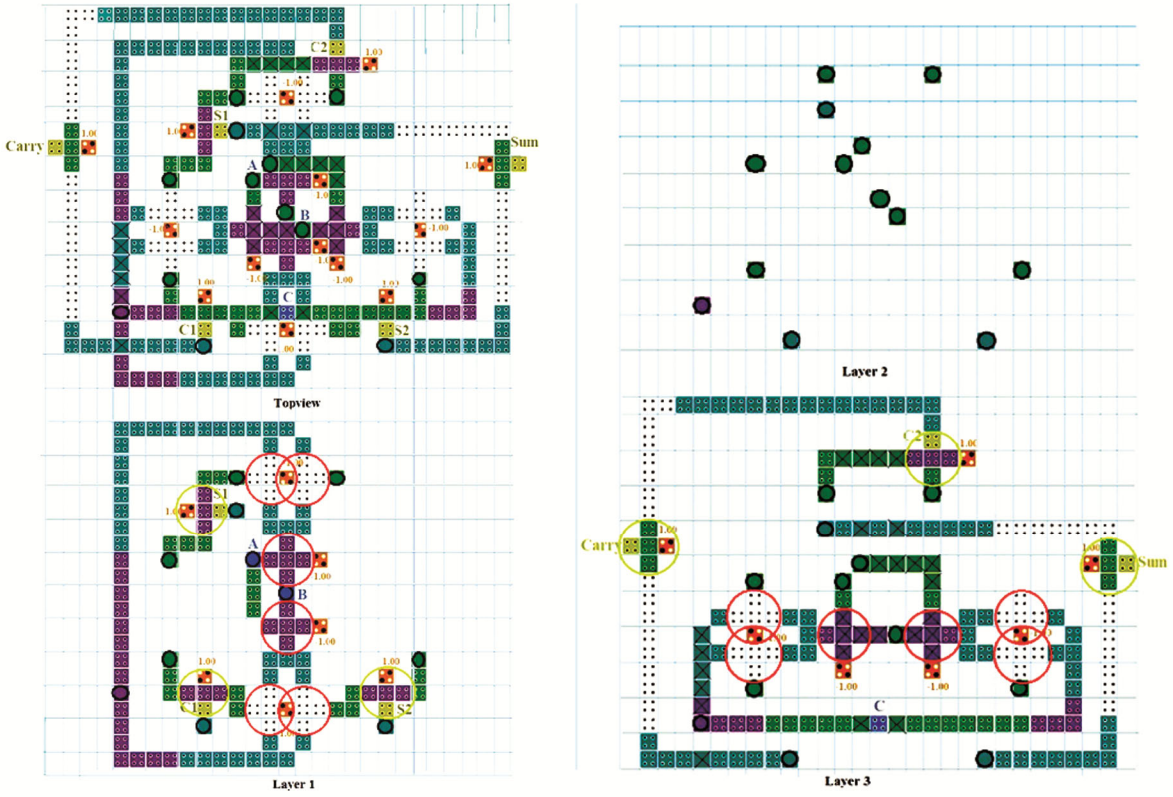

Fig. 8 — Three layer QCA architecture of PLA realizing adder function with top-view, layer 1, layer 2 and layer 3.

Layer 1 produces output functions S_1, S_2 and C_1, layer 2 possesses interconnects and layer 3 generates output functions C_2, Sum and Carry. Latency of the proposed circuit is 2.25 clock (9 clock zones).

In addition to this, the Boolean function of subtractor is also implemented here. The equation for output functions of Difference and Borrow are given in Eq. 11 and 12.

$$\text{Difference} = Y_1 + Y_2 + Y_4 + Y_7$$

$$\text{Difference} = \sum m1, m2, m4, m7 \quad \ldots (11)$$

$$\text{Borrow} = Y_1 + Y_2 + Y_3 + Y_7$$

$$\text{Borrow} = \sum m1, m2, m3, m7 \quad \ldots (12)$$

The three layer QCA architecture of PLA realizing subtractor is as shown in Fig. 10 and its operation is validated from its simulation waveform as depicted in Fig. 11. As described in adder structure, the QCA architecture of PLA, implementing subtractor

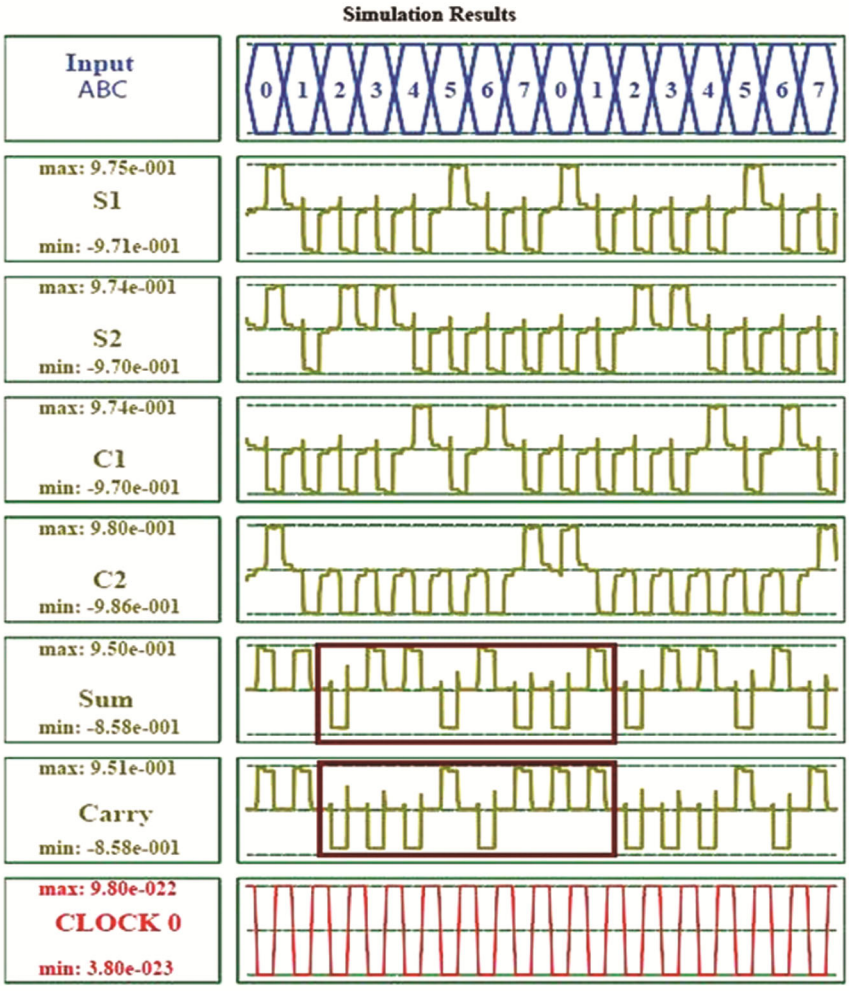

Fig. 9 — Simulation waveform for three layer PLA implementing adder function.

function is generated using 12 majority gates (marked by red circles in Fig. 10) to realize product terms or min-terms and 5 majority gates (marked by green circles) to realize sum terms. The sum terms $D_1 = Y_4 + Y_7$ and $D_2 = Y_1 + Y_2$ are obtained using two input OR gates. The final output function, Difference is generated as Difference = $D_1 + D_2$. Moreover, the final output function Borrow = $B_1 + B_2$where $B_1 = Y_1 + Y_2$ and $B_2 = Y_3 + Y_7$. In the circuit, layer 1 produces output functions D_1, D_2 and B_1, layer 2 possesses interconnects and layer 3 generates output functions B_2, Difference and Borrow. Latency of the proposed circuit is 2.25 clock (9 clock zones).

5 Comparative analysis

The QCA circuits are analyzed on the basis of performance metrics evaluated from the QCA architectures. Here, all the proposed QCA circuits are investigated and compared with previously reported circuits in the literature. Table 1 depicts the cost analysis of 2x4 decoder and its cost function (CF), area usage (A_u) is estimated using Eq. 13. and Eq.14. The cell area (C_A) is evaluated as the product of QCA cell count (Q_c) and cell area of individual cell (18nm x 18nm).

$$CF = Q_c x T_A x L_c \quad \ldots (13)$$

$$A_u = (C_A/T_A) \times 100 \quad \ldots (14)$$

The cost assessment of 2 x 4 decoder shows that the presented multilayer decoder has 55.1% better cost function as compared to the earlier reported cost-efficient circuit. The presented multilayer QCA structure of 3x8 decoder also has 51.17% better cost function than the previously reported 3x8 decoder as shown in Table 2. It is observed from these multilayer structures that the multilayer topology makes the

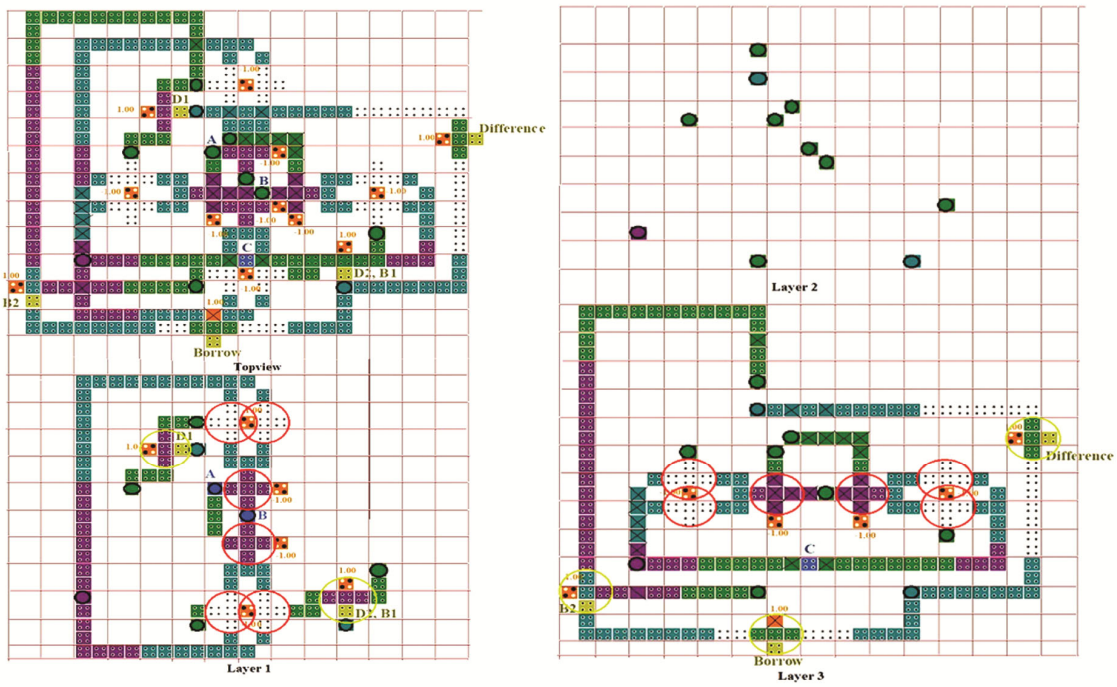

Fig. 10 — Three layer QCA architecture of PLA realizing subtractor function with top-view, layer 1, layer 2 and layer 3.

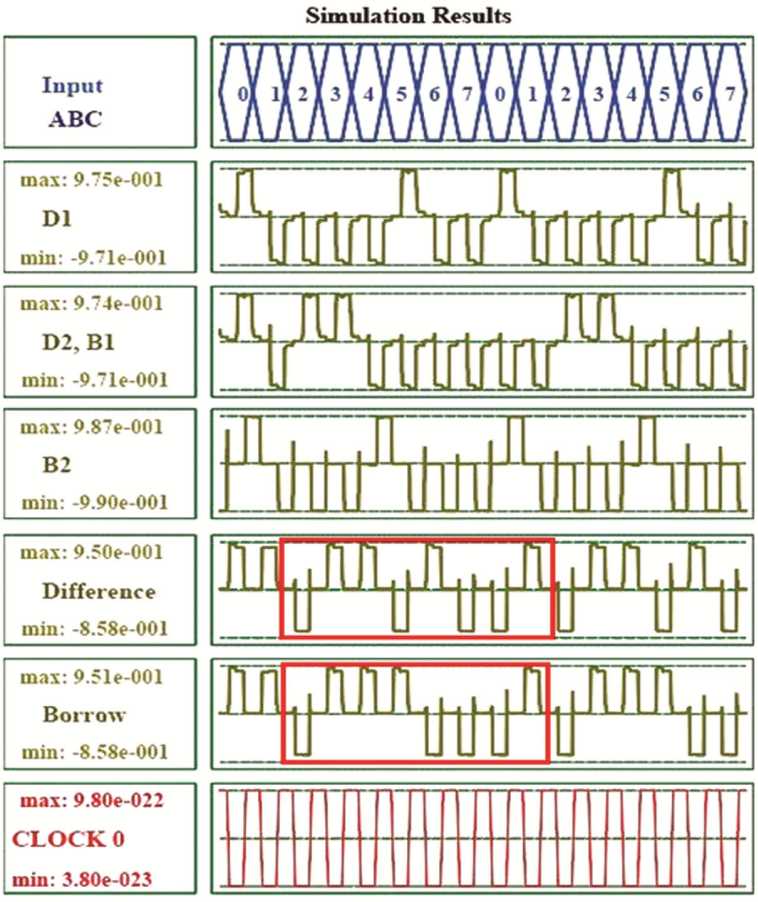

Fig. 11 — Simulation waveform for three layer PLA implementing subtractor function.

Table 2 — Cost assessment of proposed three layer 3 x 8 decoder.

3:8 Decoder	Cell count (Q_c)	Total Area (T_A) (μm^2)	Cell area (C_A) (μm^2)	Area usage (A_u) (%)	Latency (L_c)	Cost Function (CF)	% improvement
Kianpour[22]	1074	2.24	0.35	15.62	2.75	6615	99.51
De[27]	270	0.4	0.087	21.75	2.25	243	86.67
Banerjee[23]	262	0.43	0.084	19.53	1	112.66	71.24
Deng[25]	237	0.28	0.076	27.14	1	66.36	51.17
Proposed	180	0.18	0.058	32.22	1	32.4	-

Table 3 — Cost assessment of proposed three layer PLA using 3 x 8 decoder.

PLA	Cell count (Q_c)	Total Area (T_A) (μm^2)	Cell area (C_A) (μm^2)	Area usage (A_u) (%)	Latency (L_c)	Cost Function (CF)
Proposed	331	0.29	0.107	36.89	2.25	215.97

circuit more cost effective over its coplanar counterpart. Apart from area efficacy the multilayer topology gives added advantage of immunity from arbitrary interference. The proposed 3x8 decoder is further extended to design PLA which is then investigated for QCA based cost as shown in Table 3.

The cost assessment of proposed three layer PLA in Table 3 indicates that the circuit is well optimized in all the performance metrics. The designs of QCA based PLA circuits, reported in the literature are limited. Subsequently, comparative analysis is not depicted here.

6 Conclusions

This paper presents the novel multilayer designs of QCA based 2x8 and 3x8 decoders which are extended for the application of PLA. The designs are compact and cost efficient when compared with earlier reported designs. The presented 2x8 and 3x8 decoders have 55.1% and 51.17% improved cost functions respectively as compared to the existing designs. The 3x8 decoder is further extended to form PLA which is shown realizing the adder and subtractor functions. The multilayer approach is eventually used here to attain cost efficacy. The multilayer design of PLA in QCA framework is not much explored in the literature. This paper significantly contributes towards the cost efficient designs of QCA based programmable devices utilizing multilayer topology.

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