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Resistorless voltage-mode first-order allpass section using single current-controlled conveyor transconductance amplifier

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This paper presents an alternative configuration for realizing a canonical voltage-mode first-order allpass (AP) section with electronic tuning. The proposed circuit is composed of only one CCCTA and one floating capacitor, which results in a simple and resistorless structure. Its phase response can be adjusted electronically through the external dc bias currents of the CCCTA. Simulation results based on 0.35 µm BiCMOS process parameters with ± 0.75 V supply voltages are provided to demonstrate the performance of the proposed AP section.

Keywords: Current-controlled conveyor transconductance amplifier, Allpass section, Resistorless structure, Voltage-mode circuit

1 Introduction

First-order allpass (AP) filters are one of the necessary circuit blocks in many communication and instrumentation systems, where the phase linearity or group delay flatness is considered as a major design constraint[1]. This is because they are used in general for introducing a frequency dependent delay while keeping the input signal amplitude constant over the entire frequency range. For analog signal processing circuit applications, the first-order AP sections are commonly used as a fundamental circuit block to the realization of phase shifters, phase equalizers[2], oscillators[3,4] and frequency selective systems with high quality factor[5-7]. Accordingly, several attempts to implement the first-order voltage–mode AP section using different types of modern active elements can be found[4,8-19]. Many of the previously reported AP sections contain two active components[8-14]. Moreover, some of these circuits reported in Refs (4, 8, 13-14, 17-19) also have a large number of external passive components, at least three or more passive components. Among the cited references, several voltage–mode AP filter realizations employing a single active element were available[4,15-19]. However, they still require two passive components, involving external passive resistors.

Very recently, the modern active circuit block, namely the current-controlled conveyor transconductance amplifier (CCCTA), has been introduced, and its usefulness in design of analog adjustable functions has also been demonstrated[20]. This device is an extension of the conventional current conveyor transconductance amplifier (CCTA) introduced in the previous work[21], in which its x-terminal serial internal resistance (R_x) can be tuned electronically through the external biasing current. This improved feature makes the CCCTA an alternative choice for realizing electronically controllable analog signal processing circuits[20,22-23].

In our proposed approach, an alternative structure for realizing an electronically tunable voltage-mode first-order AP filter function is introduced. The proposed AP section employs a single CCCTA and one floating capacitors without using any external passive resistor, that results in canonical and resistorless structure and suitable for analog integrated circuit (IC) design. The circuit has the attractive property of electronic tuning of its phase response with a simple resistive matching. This matching condition can be easily achieved by electronic controlling of the external bias currents of the CCCTA. In order to check the proper operation of the proposed AP section, PSPICE simulation results are provided with standard 0.35 µm BiCMOS process parameters.

2 CCCTA Concept and Realization

The circuit symbol of the CCCTA is shown in Fig. 1, and its terminal relations can be described by the following matrix equation:

$$\begin{bmatrix} i_y \\ v_x \\ i_z \\ i_o \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ R_x & 1 & 0 & 0 \\ 1 & 0 & 0 & 0 \\ 0 & 0 & g_m & 0 \end{bmatrix} . \begin{bmatrix} i_x \\ v_y \\ v_z \\ v_o \end{bmatrix} \qquad \ldots(1)$$

where R_x represents the x-terminal intrinsic resistance and g_m denotes the internal transconductance of the CCCTA, respectively. Generally, both parameters R_x and g_m are controlled by electronic means. From Eq. (1), the CCCTA is characterized by high-input impedance at the y-terminal, high-output impedances at the z and o terminals, and a tunable internal resistance at the x-terminal.

Figure 2 shows the possible BiCMOS realization[23] of the CCCTA used in this work. In this structure, the x-terminal parasitic resistance (R_x) is actually dependent on the external *dc* biasing current I_A, which can be relied on the following formulation:

$$R_x = \frac{2V_T}{I_A} . \qquad \ldots(2)$$

In Eq. (2), V_T is the thermal voltage, approximately 26mV at 27°C.

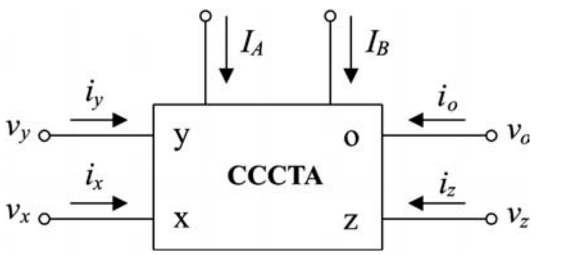

Fig. 1 — Circuit symbol of the CCCTA

From elementary small-signal circuit analysis, an effective transconductance gain (g_m) of the CCCTA derived from transconductor Q_3-Q_4 and M_5-M_6 can be written as:

$$g_m = \frac{I_B}{2V_T} . \qquad \ldots(3)$$

As shown from Eq.(3), the value of g_m is electronically adjustable by a supplied biasing current I_B.

3 Proposed Resistorless Allpass Section

Figure 3 shows the resistorless realization of a first-order voltage-mode AP section with electronic tuning property. As shown in Fig. 3, the proposed AP filter consists of only one CCCTA and one capacitor. It should be noted that the capacitor C used in the realization is floating. However, it could be implemented easily if the integrated circuit (IC) process offers a second poly layer (poly2). This

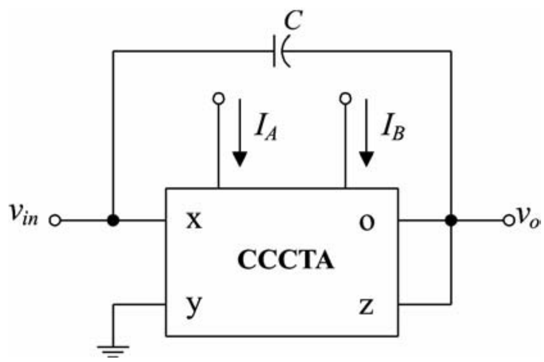

Fig. 3 — Proposed AP circuit realization

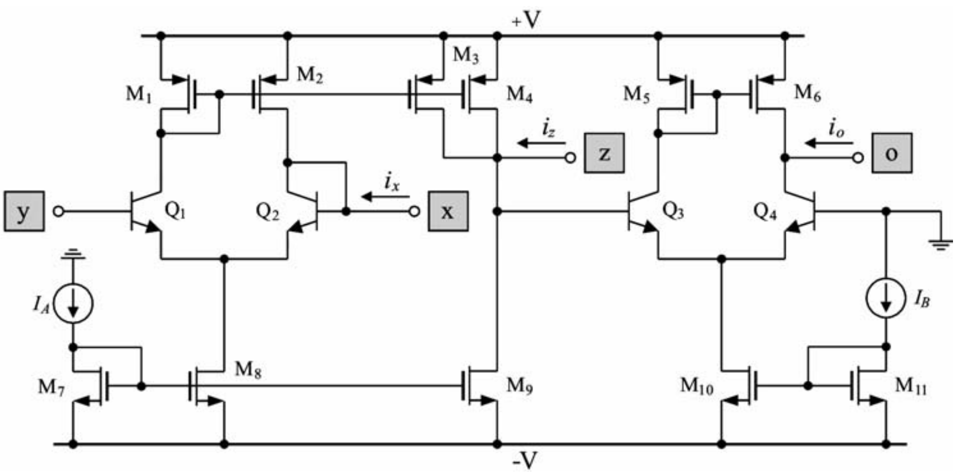

Fig. 2 — BiCMOS realization of the CCCTA

advanced IC technology enables the realization of floating capacitors as double poly (poly1-poly2) capacitors[24], which are used very commonly in analog IC designs. Thus, the canonical AP section of Fig. 3 is beneficial from the point of view of the recent integration.

Routine circuit analysis using the CCCTA property given in Eq. (1) yields the voltage transfer function of Fig. 3 in the following expression :

$$\frac{V_o(s)}{V_{in}(s)} = \frac{sC - \dfrac{1}{R_x}}{sC + g_m}. \qquad \ldots(4)$$

If the resistive condition $1/R_x = g_m$ is fulfilled, the constructed circuit of Fig. 3 performs the first-order voltage-mode AP filter with the following pole frequency (f_p) and phase response (ϕ):

$$f_p = \frac{g_m}{2\pi C}, \qquad \ldots(5)$$

and

$$\phi = \pi - 2\tan^{-1}\left(\frac{\omega C}{g_m}\right). \qquad \ldots(6)$$

Taking $I_O = I_A = I_B$ and substituting Eqs (2) and (3) into Eqs (5) and (6), the two expressions in Eqs 5 and 6 turn to:

$$f_p = \frac{I_O}{4\pi V_T C}, \qquad \ldots(7)$$

and

$$\phi = \pi - 2\tan^{-1}\left(\frac{4\pi V_T C}{I_O}\right). \qquad \ldots(8)$$

Eq. (8) indicates that the phase response adjustment of the proposed filter is achieved by electronic means through tuning I_O. In current-mode operation, equal bias currents, i.e., $I_O = I_A = I_B$, can easily be achieved by means of a basic current mirror. It is also noted that the AP configuration of Fig. 3 is not in low-output impedance, which is affected by the load impedance. Hence, to avoid this effect, an additional voltage buffer is required at the output for cascading in some applications.

4 Performance Simulation and Discussion

The PSPICE simulation program was performed to verify the functionality of the electronically tunable AP filter realization in Fig. 3. In simulation purpose, the CCCTA structure of Fig. 2 has been used with the model parameters of a standard 0.35 μm BiCMOS process. The aspect ratios of CMOS transistors were set to W/L = 7 μm/0.7 μm for the NMOS transistors and W/L = 8.5 μm/0.7 μm for the PMOS transistors. The circuit was biased with ± 0.75V *dc* supply voltages.

The circuit of Fig. 3 was designed with the following active and passive components: $I_O = I_A = I_B = 25\ \mu$A and C = 20 pF, to obtain a first-order AP voltage response with the pole frequency of $f_p \cong 3.82$ MHz. In this setting, the total power dissipation of the circuit was measured as 93.6 μW. Figure 4 shows the simulated gain and phase responses of the AP filter in Fig. 3, which is in conformity with the theory.

To evaluate the voltage swing capability of the realized AP section, the transient analysis has been performed. A sinusoidal input with amplitude value of 100 mV (peak) and frequency of 3.82 MHz was applied to the filter constructed with above mentioned active and passive component values. The time domain responses are also shown in Fig. 5. From the simulation results, at the filter output, the time shift of 63 ns was obtained, which corresponds to the phase shift of about 87°. Besides, the plot of the simulation results for the Lissajou ellipse of the proposed filter is shown in Fig. 6.

Next, to demonstrate the large signal performance, the circuit of Fig. 3 was tested by investigating the total harmonic distortion (THD) at the output for sinusoidal input signals of 1.53 MHz and 3.82 MHz. Figure 7 shows the dependence of THD (%) on the

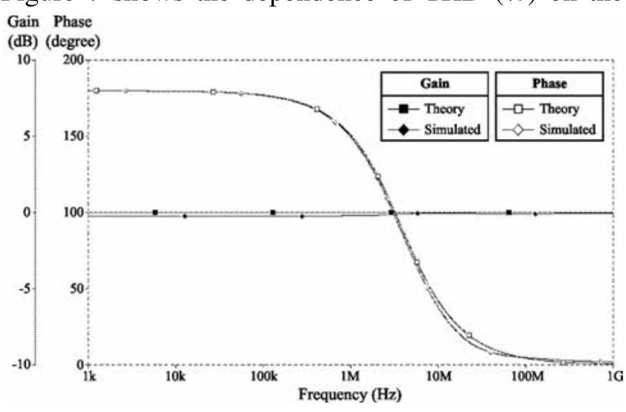

Fig. 4 — Theory and simulated gain and phase responses for the AP filter in Fig.3 at the pole frequency

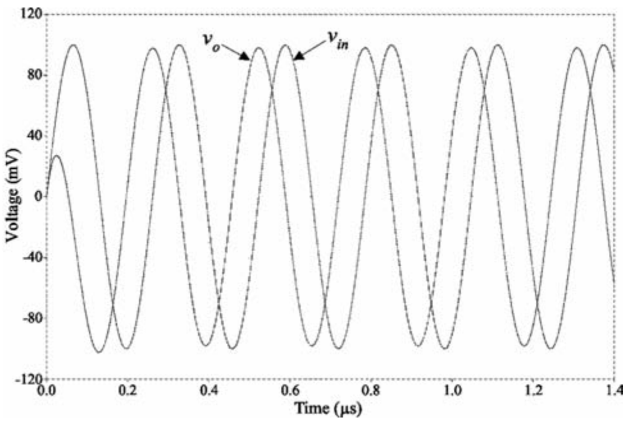

Fig. 5 — Time domain responses for the AP filter in Fig.3 at the pole frequency

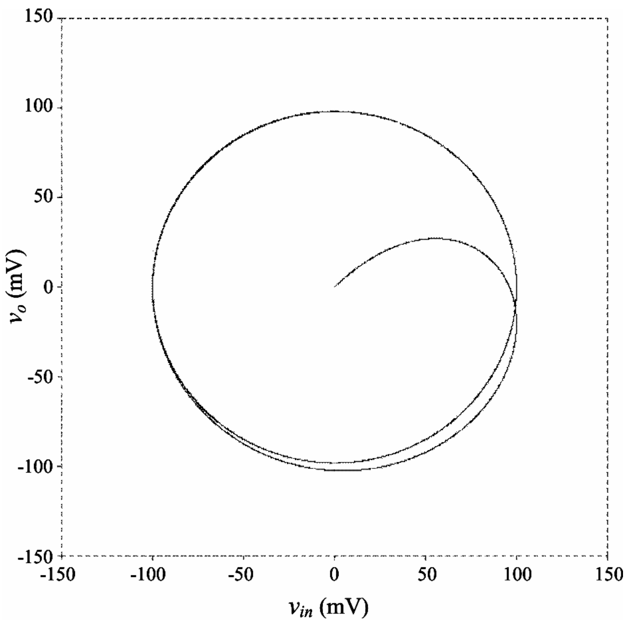

Fig. 6 — Simulation result for Lissajou ellipse at the pole frequency

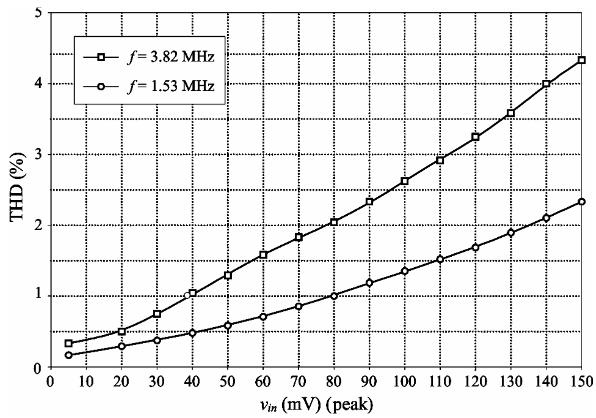

Fig. 7 — THD variation against input signal amplitude

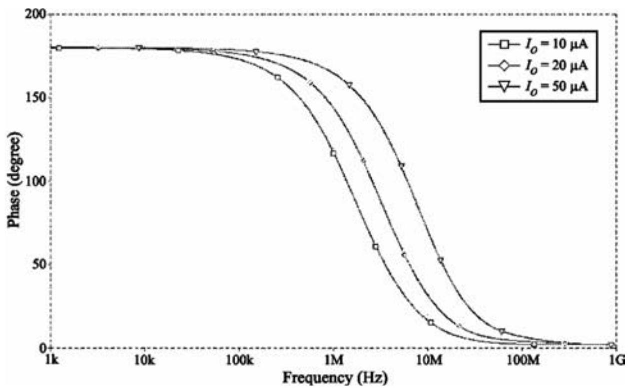

Fig. 8 — Electronic f_p tuning as a function of I_O

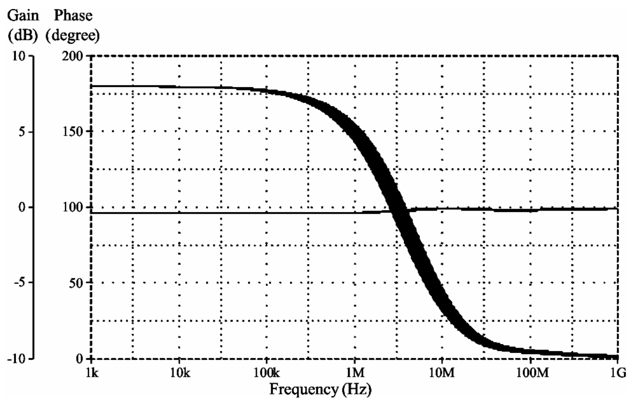

Fig. 9 — Monte-Carlo simulations of the phase and gain responses for 10% Gaussian deviation in C value

input voltage signal level for the designed values as given above. It can be observed that the THD value at f = 3.82 MHz is found to be less than 4.5% for the signal amplitude below 150 mV (peak), and the THD value is below 2.4% at f = 1.53 MHz.

Furthermore, the electronic controllability of the proposed circuit is shown in Fig. 8, where the corresponding phase responses with respect to the bias current I_O are given. The pole frequency f_p is varied from 1.50 MHz, 2.95 MHz to 7.45 MHz for a variation of I_O from 10 μA, 20 μA, to 50 μA, respectively.

In our proposed circuit, the statistical analysis has also been performed for robustness using Monte-Carlo simulation. After 200-simulation runs, Monte-Carlo analysis for 10% Gaussian deviation in the value of the capacitor C, and in the values of g_m and R_x are given in Figs 9 and 10, respectively.

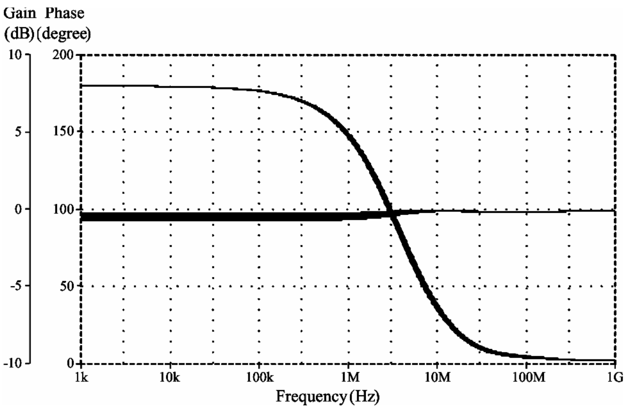

Fig. 10 — Monte-Carlo simulations of the phase and gain responses for 10% Gaussian deviation in g_m and R_x values

The Monte-Carlo statistical analysis results given in Fig. 9 reveal that, due to the deviation in the C value, the phase response of the filter is affected in the range of –4.23% ~ +5.16%. In Fig. 10, the gain response changes by 0.45 dB in the operating frequency of 1 kHz ~ 1 MHz. As seen from these plots, the proposed circuit works well against uncontrollable random variation in component values, which is reasonable sensitivity performance.

5 Comparison with the Existing Voltage-Mode AP Sections

At this point, it is useful to compare the proposed circuit of Fig. 3 with other previously reported first-order voltage-mode AP sections given in

Table 1 – Performance comparison between the existing first-order voltage-mode AP sections and the proposed circuit

Circuits [Ref.]	Features							
	No. of active elements	No. of passive elements	Technologies	Supply voltages	Electronic control	Resistorless structures	Matching condition requirement	THD
[4]	CDBA = 1	R = 2, C = 2	AD844	±12V	no	no	yes	N/A
[8]	CCII = 2	R = 2, C = 2	AD844	±12V	no	no	yes	N/A
[9]	CCCII = 1, OA = 1 CCCII = 1, OA = 1 CCCII = 2	C = 2 C = 2 C = 1	Bipolar array ALA400, OP-27	±2.5V	yes	yes	yes	N/A
[10]	DVCC = 2	C = 1	0.5μm CMOS	±2.5V	no	yes	no	N/A
[11]	OTA = 1, D = 1	C = 1	TSMC 0.35μm	±2.5V	yes	yes	no	~ 0.3% (@ f = 100 kHz)
[12]	UVC = 1, OTA = 1	C = 1	Bipolar array ALA400, OP-27	±2V	yes	yes	no	N/A
[13]	DVCC = 1, OTA = 1	MOS conductor = 2, C = 1	0.5μm MOSIS	±0.747V, ±1.65V	yes	no	no	~ 1.85% (@ f = 100 kHz)
[14]	DVCC = 2	R = 2, C = 1	0.5μm CMOS	±2.3V	no	no	yes	~ 3.7% (@ f = 1.59 MHz)
[15]	DDCC = 1	R = 1, C = 1	0.5μm MIETEC	±2.5V, +1.7V, -1.3V	no	no	no	~ 1.6% (@ f = 1 MHz)
[16]	CDBA = 1 CCCDBA = 1	R = 3, C = 1 R = 1, C = 1	Bipolar array ALA400	±2.5V	yes	no	yes	N/A
[17]	MCCII = 1	R = 2, C = 1	TSMC 0.35μm	±2.5V	no	no	yes	N/A
[18]	DO-CCII = 1	R = 2, C = 1	TSMC 0.35μm	±1.5V	no	no	yes	~ 1% (@ f = 439 kHz)
[19]	FDCCII = 1	R = 2, C = 1	TSMC 0.35μm	±3.3V	no	no	yes	~ 4.27% (@ f = 1.59 MHz)
Proposed circuit	CCCTA = 1	C = 1	0.35μm BiCMOS	±0.75V	yes	yes	no	< 4.5% (@ f = 3.82 MHz), < 2.4% (@ f = 1.53 MHz)

CCII = Second-Generation Current Conveyor, CCCII = Current-Controlled Current Conveyor, DVCC = Differential Voltage Current Conveyor, DDCC = Differential Difference Current Conveyor, MCCII = Modified CCII, DO-CCII = Dual-Output Second-Generation Current Conveyor, FDCCII = Fully Differential Second-Generation Current Conveyor, OA = Operational Amplifier, OTA = Operational Transconductance Amplifier, D = Differential Amplifier, UVC = Universal Voltage Conveyor, CDBA = Current Differencing Transconductance Amplifier, CCCDBA = Current-Controlled Current Differencing Transconductance Amplifier

Refs (4, 8-19). The performance comparison of the proposed circuit with the recent ones is provided in Table 1. With respect to the circuits given in Refs (4, 8-19), the proposed circuit uses lower *dc* supply voltages; this in turn consumes lesser power. When compared to the previous works realized with active and passive components, the proposed circuit uses fewer components which would save much of occupied chip area. As compared with Refs (11, 13-15, 18, 19), the variation of THD (%) of the proposed circuit is found lower for a high-frequency operation.

6 Conclusions

An electronically tunable voltage-mode first-order AP filter realization using a recently modified active element, the CCCTA has been described in this work. The proposed AP section is constructed using only a single CCCTA and one capacitor, which is suited for advanced IC implementation. It is canonical and resistorless. Moreover, its phase response is tunable by adjusting the bias currents of the CCCTA. The performance of the proposed circuit is verified by PSPICE simulation using a BiCMOS realization of CCCTA.

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