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Robust Logic Circuits Design Using SOI Shorted-Gate FinFETs

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The scaling of planar Metal Oxide Semiconductor Field Effect Transistor (MOSFET) technology has reached to its extremity. Double Gate (DG) device was introduced to derive the benefits of scaling gate lengths. Fin-shaped Field Effect Transistors (FinFETs) proved to be the best architecture to realize a double gate structure. In this paper, a static leakage control technique is proposed and a ring-oscillator of five inverters based on shorted gate (SG) FinFETs is simulated using the technique. The basic logic gates like Inverter, 2-input NAND gate, and 2-input NOR gate are simulated using the proposed technique. Leakage power and Power Delay Product (PDP) optimization of 93.46% and 97.78% has been found in 2-input SG FinFET-based proposed NAND gate compared to that of 2-input SG FinFET-based conventional NAND gate. Also, SG FinFET-based proposed 2-input NOR gate shows 98.03% and 98% optimization of leakage power and PDP, respectively compared to the SG FinFET-based conventional 2-input NOR gate. The proposed SG FinFET-based ring-oscillator shows a leakage power and PDP optimization of 62.12% and 35.56%, respectively in comparison to the conventional SG FinFET-based ring-oscillator. The reliability of the proposed circuit is calculated, which came out to be the highest at 0.7V supply and 16nm process node for a 10% deviation in operating parameters. Also, the process parameter variation of leakage power, delay, and PDP of the proposed circuit came out to be proper and stable thus maintaining the functionality of the proposed circuit.

Keywords: Nanoelectronics; SG FinFET; GLBB; LCNT; Reliability; Monte-Carlo

1 Introduction

The need for the introduction of low-power design techniques is inevitable in battery-operated portable devices. Underneath 45nm process technology, the standby power contributes to more than half of the total power consumption in an Integrated Circuit (IC)[1]. The gradual channel approximation, which is one-dimensional, does not report any subthreshold current. In MOSFETs, when the gate to source voltage (V_{GS}) is less than the threshold voltage (V_{th}) then charge carriers have to cross a potential barrier whose magnitude is a function of V_{GS} only. When the short channel effects (SCE) become conspicuous, this barrier potential shows a dependence on the drain to source voltage (V_{DS}) as well. An increase in V_{DS} reduces the potential barrier thus allowing the drain current to flow in the threshold region[2]. The static power dissipation is the leakage power that the transistor manifests in the subthreshold region of operation and is represented as I_{SUB} or I_{OFF}[3]. This I_{OFF} hampers further downscaling of V_{th}.

In MOSFETs, a very high I_{ON}/I_{OFF} is desired. A small V_{th} is required to get a higher I_{ON} as it is proportional to $(V_{GS} - V_{th})^2$.The scaling of V_{th} offers a trade-off between theI_{ON} and I_{OFF} as decreasing the V_{th} increases I_{OFF}[4]. The surface potential throughout the channel doesn't vary under weak inversion. The lateral concentration gradient causes the diffusion of minority carriers which leads to subthreshold current flow under weak inversion. There is an exponential relationship of I_{OFF} with V_{GS}[5]. When V_{gs} is lower but close to V_{th}, the subthreshold current or I_{OFF} becomes remarkable and the magnitude of power consumption due to this leakage becomes approximate to that of switching power dissipation. The expression for I_{SUB} is given in Eq. 1.

$$I_{SUB} = I_0(exp\,|(V_{GS} - V_{th0} - \eta V_{DS} + \gamma V_{BS})/\eta V_T|).\ (1 - exp^{|-V_{DS}/V_T|}) \quad \ldots (1)$$

Where,

$$I_0 = \mu C_{ox}.W/L.{V_T}^2 exp|1.8| \text{ and } V_T = KT/q \quad \ldots (2)$$

Where, μ, C_{ox}, and W/L denote carrier mobility, oxide capacitance, and aspect ratio of MOSFET, respectively. V_T and V_{th0} denote thermal voltage and threshold voltage at zero body bias, respectively. In Eq. 1, η specifies the barrier lowering coefficient and γ is the body effect coefficient[5]. Eq. 1 shows the exponential dependence of subthreshold current on both gate and drain voltages leading to an SCE called

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drain-induced barrier lowering (DIBL). Relentless scaling of the planar devices forced the IC industry to rethink and reform the conventional transistor architecture and manufacturing technology. As the design rules continued to shrink from micrometers to a few nanometers, SCEs continued to dominate the MOSFET subthreshold region leading to more and more leakage.

The concept of FinFETs was first reported by Berkeley University as a transistor with Silicon on insulator (SOI) substrate in the year 1999. After a gap of more than a decade, Intel fabricated it into technology putting it into use in the first Ivy bride processor at 22nm process technology node. FinFETs are non-planar multi-gate transistors in which the gate region protrudes out of the substrate to form a non-planar structure[6]. Silicon fin lies upright on the bulk/SOI substrate. Fin nitride is deposited above the silicon fins as a thin pad oxide for protection during etching. The gate oxide layer is used to form the gates from the vertical sides of the fin. The threshold voltage is adjusted by the modification of the gate work function[7].

The critical device dimensions of the FinFETs include device length (L), fin-width (F_W), fin-height (F_H), and fin-thickness (F_T). All the terminals which include the source, drain, gate, and substrate are part of the fin structure. The position of these terminals is determined by the location of the gate terminal against the fin. Gate is placed vertically to the fin plane and encloses the fin on multiple sides, a maximum of four sides. The portion of the fin underneath the gate is the channel. The extra portions of the fin which don't lie underneath the gate form the interchangeable source and drain terminals of FinFET. Oxide isolation using an oxide layer of thickness t_{ox} is provided between the gate and fins[8]. The width of the fin is the same as the channel width and L is the length of polysilicon material encasing the fin[9].

DG and tri-gate FinFETs are non-planar devices, where the gate encloses the fin from two and three sides, respectively. F_H is the only parameter that determines the F_W in DG FinFETs as F_W equals to twice of F_H. In tri-gate devices, both F_H and F_T determine the F_W where later equals the summation of twice of F_H and F_T ($F_W = 2F_H + F_T$). Besides the two sides, current flow in tri-gate devices has also been observed from the top side of the fin[10]. Fig. 1 shows a three-dimensional structure of FinFET.

As current flows through the fins, F_W determines the current drive capability of FinFETs[11]. F_W is increased mostly by increasing F_H as F_T doesn't have much impact on the device width. F_T can also be increased while maintaining the condition of $F_T \ll L$ to keep SCEs in check as it administers the subthreshold swing. Multiple fins can be designed to increase F_W hence improving the current drive in FinFETs. Multiple channels are created due to the use of multiple fins as each fin contributes to an individual channel[12]. Using the n-number of fins, the effective channel width equals to $F_W = n(2F_H + F_T)$.

Device width in FinFETs is quantized and is an integer multiple of F_H[13]. For a chip designer, the increments to device widths available are determined by the size of the fins. In contrast to this, the unrestricted availability of device widths in planar devices allows designers to achieve any desired tradeoff in power and performance. The device width quantization can prove to be a barrier to the widespread adoption of the technology beyond 7nm. The tri-gate structure provides some relaxation as the fin can be made narrower or wider from the top to obtain the appropriate device width.

FinFET working is governed by the same equations as that of planar devices. If V_{DS}, V_{GS}, and V_{FB} represent the drain to source, the gate to source, and flat band voltage in an n-channel DG FinFET. If $V_{GS} < V_{FB}$, the device doesn't conduct and at $V_{GS} > V_{FB}$, channel inversion takes place. After the channel is inverted if $V_{GS} < V_{DS-SAT}$, the device is in the linear region, and if $V_{DS} > V_{DS-SAT}$, the device is in the saturation region. The drain current in the linear region in a DG FinFET is given by Eq. 3.

$$I_D = 2\mu(W/L)C_{ox}[(V_{GS} - V_{th} - V_{DS}/2)V_{DS}] \quad \ldots (3)$$

The expression for drain current in linear mode is the same as that of planar devices with the multiplication of two, which reflects that the current is flowing from the two sides of the fin.

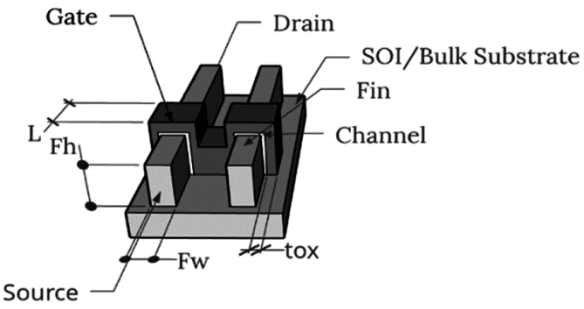

Fig. 1 — 3-D structure of FinFET.

V_{th} in expression 3 is given by the Eq. 4.

$$V_{th} = V_0 + 2V_T \ln|V_{GS} - V_0/4rV_T| \quad \ldots (4)$$

V_0 in Eq. 4 is given by the Eq. 5.

$$V_0 = V_{FB} + 2V_T ln|2/F_T|(2 \in_{si} V_T/qn_i)^{1/2} \quad \ldots (5)$$

The quantity represented by r is given by Eq. 6.

$$r = \in_{si} t_{ox}/\in_{ox} F_T \quad \ldots (6)$$

For DG FinFETs in saturation mode ($V_{DS} > V_{DS-SAT}$), the drain current is given by Eq. 7.

$$I_{D-sat} = \mu_s.W/L.C_{OX}\left[(V_{GS} - V_{th})^2 - 8rV_T{}^2.exp|V_{GS} - V0 - VDS/VT \right. \quad \ldots (7)$$

Sub threshold leakage current is the current which flows before the FinFET turns ON and is present for V_{GS} values less than V_{FB}. In DG FinFETs, the sub threshold current is given by Eq. 8.

$$I_{sub} = \mu.W/L.KTF_T.exp|V_{GS} - V_{FB}/V_T|.(1 - exp|V_{DS}/V_T|) \quad \ldots (8)$$

FinFETs have an ultra-thin body and keeping the values of F_T low helps the designer to minimize the leakage current[14]. FinFETs are fabricated over either SOI or bulk substrate. FinFETs come in several variants like SG FinFETs, independent gate (IG) FinFETs, low power (LP) FinFETs, and hybrid FinFETs[15]. SG FinFETs have back and front gates shorted making them three-terminal devices like MOSFET. IG FinFET is a four-terminal device, where two gates can be biased independently. LP FinFETs show high delay and least leakage and offer low performance compared to SG FinFETs and IG FinFETs. Hybrid FinFETs possess the characteristics of both SG and IG FinFETs.

An odd numbered inverter chain is used as an inverting circuit which gives a particular delay. The inverter is the base circuit for constructing the Ring-Oscillator[16]. By connecting the output of the last inverter to the first inverter, a Ring-Oscillator can be formed. The frequency requirements of the oscillator decide the number of inverters used to design it. Compared to the single inverting amplifier, the gain in the Ring-Oscillator is more. The higher the number of inverters used to design the Ring-oscillator, the lesser will be the frequency output of the oscillator as each inverter gives a delay that is cumulative[17]. Ring-Oscillators are used in applications that include measuring the consequences of process variations in wafers during their manufacturing, as frequency synthesizers, in serial data communication for data recovery, as voltage-controlled oscillators in phase locked loops, and much more.

This paper dispenses a novel reliable and robust low-power technique. Some basic CMOS gates and a 5-Inverter stage Ring-oscillator are simulated using the proposed technique using both CMOS and SG FinFET technology. Operating point analysis, reliability analysis, and process variations have been carried out.

The rest paper is arranged as: Section 2 describes the literature review of leakage control methods. Section 3 presents the proposed technique. Section 4 explains the results and discussion in which section 4.1 carries out the operating point analysis and section 4.2 deals with the reliability analysis. In section 5, conclusion of the work has been carried out.

2 Previous Related Work

Many static leakage control techniques have been proposed in the past. At circuit level, the leakage control techniques include dynamic threshold (DT) CMOS[18], multi-threshold (MT) CMOS[19], ONOFIC[20], modified ONOFIC[21], leakage control NMOS transistor (LCNT)[22] and gate level body bias (GLBB)[23]. In DTCMOS, both low and high threshold transistors are used to improve the power delay product of the circuits. Low threshold transistors maintain the performance while the high threshold transistors control the static leakage. Critical paths are conducting paths through which logic passes while non-critical paths are non-conducting paths in a circuit. High threshold transistors are reserved for non-critical paths while the low threshold transistors are allocated in critical paths. Transistors form a stack in critical paths which leads to static leakage reduction.

In MTCMOS, multiple threshold transistors are employed to reduce the leakage in standby mode and enhancing the performance in active mode. This technique is also called the sleep transistor method as high V_{th} sleep transistors put the circuit in standby or sleep mode. High V_{th} sleep transistors are placed near VDD (header) or ground (footer). The header transistor is turned ON when the sleep signal is low while the footer is turned ON when the sleep signal is high. This configuration cuts off the logic block from the power rails during the standby mode hence curbing the leakage. ONOFIC was proposed to overcome the difficulty of implementing the different threshold voltages in DTCOMS and MTCMOS techniques. ONOFIC block consists of an NMOS and a PMOS in such a way that the drain of PMOS is

connected to the gate of NMOS while the gate of PMOS is connected to the output. This ONOFIC block is inserted between the pull-up and pull-down networks. Logic is passed to the ground when the ONOFIC block is turned ON and the block is turned OFF when output is logic high.

Another low-power approach is the LCNT technique where two NMOS leakage control transistors are inserted in series between the pull-up network (PUN) and pull-down network (PDN) with the gates of two NMOS transistors connected to the output node. So, the voltage at the output controls the switching of these two NMOS transistors forming a stack. The logical arrangement of the LCNT technique is shown in Fig. 2.

In the GLBB technique, logic is operated by a logic sub-circuit, and the body voltage of all the devices are provided by the Body Bias Generator (BBG) circuit. BBG consists of an NMOS in the pull-up and a PMOS in the pull-down. When V_{OUT} is at logic high, body bias voltage (V_B) is high which prepares the pull-down network for faster switching. The logical arrangement of the GLBB technique is shown in Fig. 3

3 Proposed Design

As propagation delay and power dissipation are the crucial parameters, the need for optimizing the PDP has led to the proposition of many leakage power techniques. This paper presents a power-efficient technique to reduce the static power to keep the PDP optimized. The proposed design has an extra SG-PFET and a SG-NFET transistor connected in series between PUN and PDN.The second gate terminal of both N-type and P-type FinFET is shorted to represent them as SG FinFET transistors. The logical arrangement of the proposed low power technique is shown in Fig. 4. The source of XMP is connected with PUN, and the gate of XMP is connected with the input terminal. The drain of XMP, the gate of XMN, and the drain of XMNare connected to the output. The source of XMN is connected with the PDN.

An inverter using the SG FinFET transistors has been designed using this technique to account for the proper logic functionality and leakage power by the proposed inverter in comparison to the inverter designed using other techniques. The circuit diagram of the proposed SG FinFET-based inverter is shown in Fig. 5. When the input is at logic zero, XMP1 and XMP2 are ON while XMN1 and XMN2 are OFF so, the output node is charged to VDD. The proposed technique utilizes the concept of stacking to attain low static power.

When more than one transistor in a stack is OFF then there is a decrease in the leakage current flowing

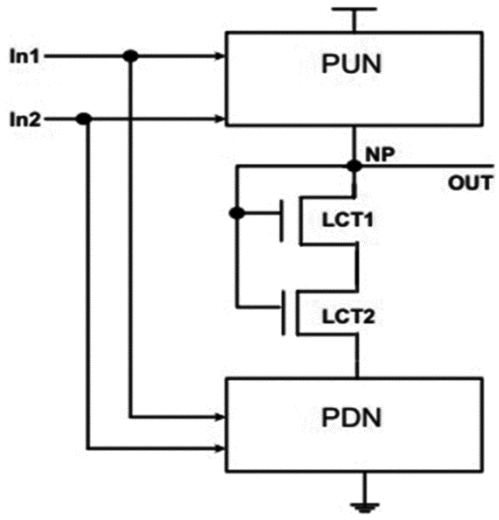

Fig. 2 — LCNT logic.

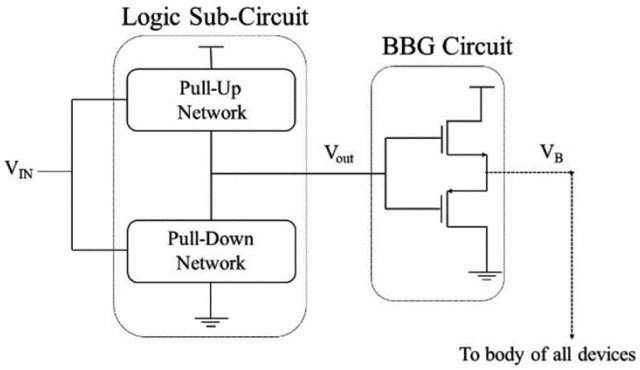

Fig. 3 — GLBB logic.

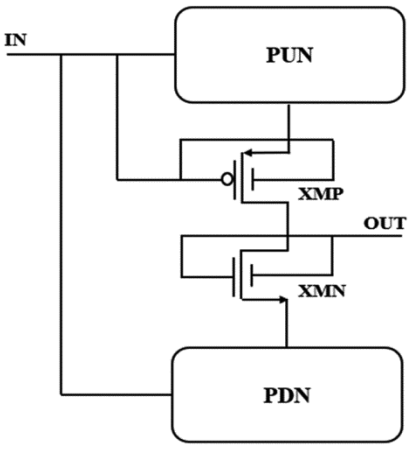

Fig. 4 — Logical arrangement of the proposed low power circuit technique.

through a series connected transistors in a stack. XMP1 and XMP2 form a stack. A P-channel FinFET shows an exponential increase in I_{SUB} when V_{SG} is increased. When XMP1 is OFF, the source of XMP2 is at a voltage less than VDD, so V_{SG} of XMP2 becomes negative. This negative V_{SG} as shown in the Eq. 1 indicates a decrease in I_{SUB} in static mode.

When the input is at logic high, XMP1 and XMP2 are OFF while XMN1 and XMN2 are ON which discharges the output node to the ground thus maintaining the functionality of an inverter.

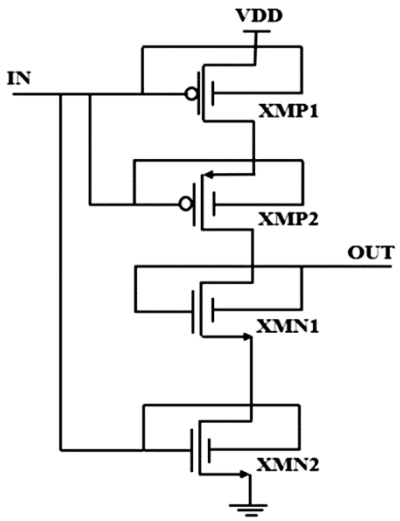

Fig. 5 — SG FinFET-based inverter using the proposed technique.

Transient analysis of the SG FinFET-based inverter has been carried out at a 16nm process node and a VDD of 0.7V using the T-Spice tool. Transient characteristics of the proposed SG FinFET-based inverter are shown in Fig. 6. The output of the inverter yields proper high logic as 700mV and a low logic of 0V.

The Ring-Oscillator has been used as a benchmark and the proposed Ring-Oscillator is designed by connecting the proposed SG FinFET-based inverters in back-to-back topology in the form of an inverter chain as shown in Fig. 7.

Input pulse is given at the first inverter and output is taken from the fifth or last inverter. The operating point analysis of the proposed circuit is compared with that of conventional CMOS Ring-Oscillator, conventional SG FinFET-based Ring-Oscillator, LCNT, and GLBB-based Ring-oscillators using SG FinFET transistors only. Inverting characteristics of the odd-numbered based inverter chain is maintained as shown by the transient characteristics in Fig. 8. The output high and low logic is properly maintained at the output. Also, the leakage power of the proposed Ring-Oscillator has been calculated as the sum of leakage powers at logic low and high of the input signal, which came out to be lower than that of the conventional Ring-oscillator and Ring-Oscillators designed by other low-power techniques.

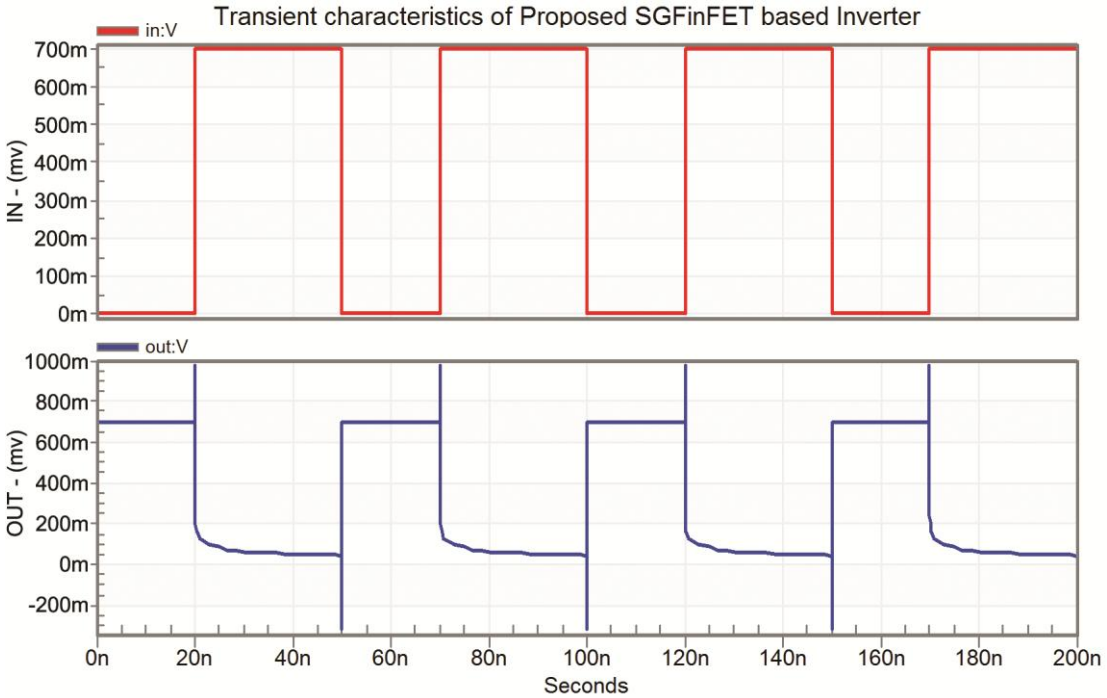

Fig. 6 — Transient characteristics of the proposed SG FinFET-based inverter.

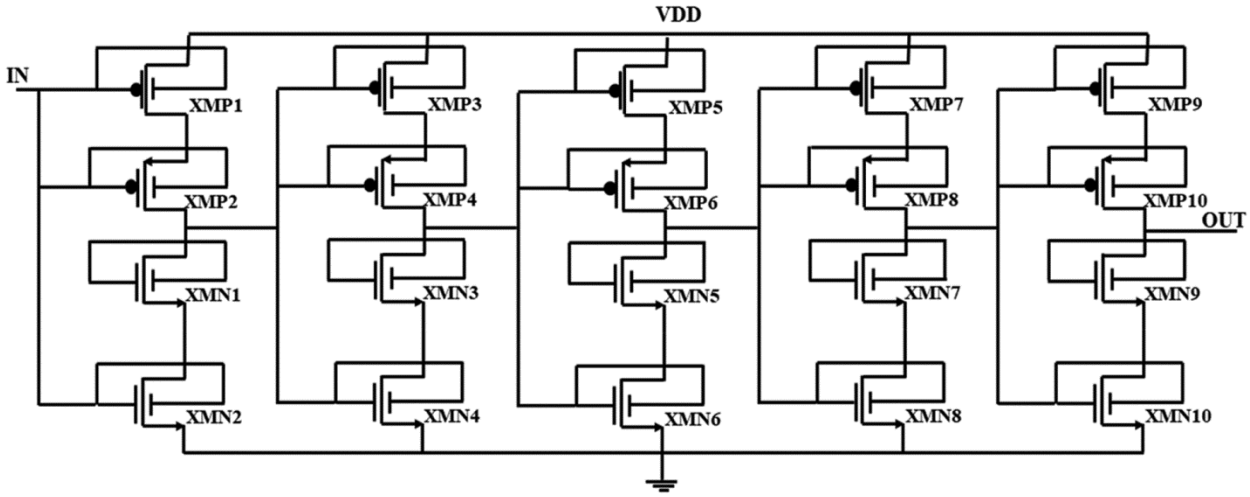

Fig. 7 — SG FinFET-based Ring Oscillator using 5 inverters.

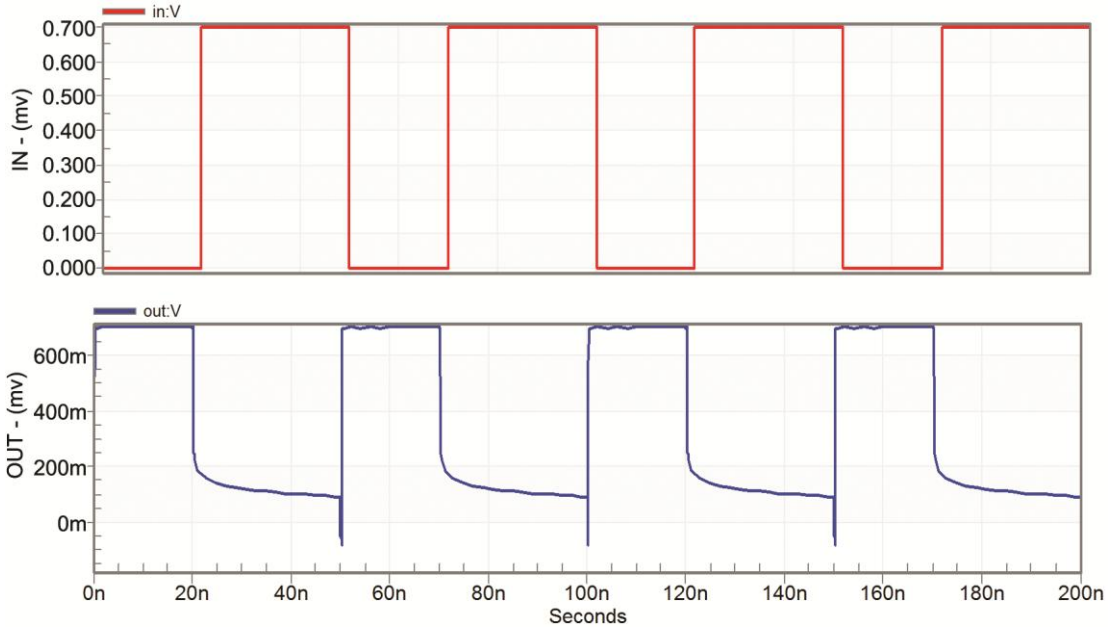

Fig. 8 — Transient characteristics of SG FinFET-based Ring-Oscillator.

4 Results and Discussion

Low standby power predictive technology model for multi-gate transistors at 16nm process node is used to simulate the circuits using SG FinFET transistors. Fin-pitch (F_P), F_T, F_H, T_{ox}, and gate length (L) of the used transistors are 42nm,12nm, 26nm, 1.5nm, and 20nm, respectively.

4.1 Operating Point Analysis

Using the proposed technique, Inverter, 2- input NAND, and 2-input NOR gates are simulated using the conventional (Conv.) CMOS design and the leakage control techniques like LCNT and GLBB. For comparative analysis, these circuits are simulated using both the CMOS and SG FinFET transistors. Leakage power, propagation delay, and PDP of the circuits are computed and compared with those of the circuits implemented using the proposed technique.

Table 1 shows the leakage power, delay and PDP of the simulated circuits. Delay is taken as the highest of delays during the two logics. The leakage power of the proposed inverter simulated using the SG FinFETs transistors is minimum followed by the conventional inverter simulated using SG FinFETs. The proposed CMOS-based inverter shows lower leakage power and PDP compared to that of a conventional CMOS

Table1 — Operating point analysis of inverter, 2-input NAND, and 2-input NOR gates

Technique	Leakage Power (W)	Delay (s)	PDP (zJ)
	Inverter		
Conv. CMOS	29.97n	1.57p	47.05
GLBB CMOS	76.85 µ	1.93p	1.48×10^5
LCNT CMOS	1.43n	49.94n	7.14×10^4
Conv.FinFET	30.2p	4.13p	0.124
Proposed CMOS	249.25p	4.89p	1.22
GLBB FinFET	65.83 µ	2.04p	1.34×10^5
LCNT FinFET	56.68p	20.02n	1121.12
Proposed FinFET	9.48p	9.45p	0.089
	2-Input NAND gate		
Conv. CMOS	58.83n	5.59p	328.85
GLBB CMOS	332.12 µ	5.11p	16.9×10^5
LCNT CMOS	2.5n	313.47p	783.67
Conv.FinFET	56.12p	18.56p	1.04
GLBB FinFET	102.85 µ	4.24p	4.3×10^5
LCNT FinFET	12.54p	3.650n	45.77
Proposed CMOS	171.14p	7.62p	1.3
Proposed FinFET	3.67p	6.49p	0.023
	2-Input NOR gate		
Conv. CMOS	40.58n	1.09p	44.23
GLBB CMOS	168.36 µ	1.20p	2.02×10^5
LCNT CMOS	6.362n	2.46p	15.65
Conv.FinFET	95.35p	1.09p	0.1
GLBB FinFET	128.93µ	1.53p	1.97×10^5
LCNT FinFET	30.03p	12.30n	369
Proposed CMOS	32.02p	4.54p	0.14
Proposed FinFET	1.87p	1.1p	0.002

inverter and offers a PDP reduction of 97.41%. The effect of stacking employed in the proposed technique resulted a decrease in I_{SUB} which is a major source of leakage power at 16nm. Efficient control of SCEs in FinFETs also leads to the reduction of leakage power in FinFET-based circuits. SG FinFET-based proposed inverter shows a leakage power reduction of 68.60% compared to SG FinFET-based conventional inverter. The leakage power of the SG FinFET-based 2-input NAND gate is the lowest followed by LCNT SG FinFET-based 2-input NAND gate. The PDP of the proposed SG FinFET-based 2-input NAND gate is minimum followed by the SG FinFET-based conventional 2-input NAND gate. SG FinFET-based proposed 2-input NAND gate shows 93.46% and 97.78% optimization of leakage power and PDP, respectively compared to the SG FinFET-based conventional 2-input NAND gate. Similarly, leakage power and PDP shown by the SG FinFET-based proposed 2-input NOR gate is minimum followed by the SG FinFET-based LCNT 2-input NOR gate.

SG FinFET-based proposed 2-input NOR gate shows 98.03% and 98% optimization of leakage power and PDP, respectively compared to the SG FinFET-based conventional 2-input NOR gate. Operating point analysis of SG FinFET-based Ring-Oscillator simulated using various techniques is shown in Table 2.

Table 2 — Operating point analysis of SG FinFET-based Ring-Oscillator

Technique	Power (W)	Delay (ps)	PDP (J)
Conventional	187.84n	13.82	2.59a
GLBB (CMOS-based)	62.5µ	12.96	8.10f
LCNT (CMOS-based)	34.66µ	111.4	3.86f
Conv (SG FinFET-based)	156.49p	40.96	6.41z
GLBB (SG FinFET-based)	13.39 µ	15.78	21.93a
LCNT (SG FinFET-based)	9.06 µ	184.9	1.675f
Proposed (CMOS-based)	14.61n	73.35	1.07a
Proposed (SG FinFET-based)	59.28p	69.8	4.13z

Power dissipation of the Ring-Oscillator designed by various techniques has been calculated by the addition of power dissipations at logic low and high. The delay is taken as the maximum of the delays in the two transitions. The leakage power and PDP reduction of 92.22% and 58.68%, respectively are in the CMOS-based proposed Ring-Oscillator compared to that of conventional CMOS-based Ring-oscillator. There is a power and PDP reduction of 62.12% and 35.56%, respectively in the SG FinFET-based proposed Ring-Oscillator compared to that of the SG FinFET-based conventional Ring-Oscillator. The delay of the proposed Ring-Oscillator is more than that of the conventional one due to the use of extra transistors but the overall energy efficiency of the proposed Ring-Oscillator is higher. The GLBB and LCNT-based Ring-Oscillators are less efficient in terms of leakage power and energy per switching event as compared to the proposed Ring-Oscillator.

4.2 Reliability Analysis

Reliability is another important aspect of low-power design that needs to be taken care of. Due to the relentless scaling of transistors, reliability issues due to the variation in transistor parameters occur at lower nodes. Reliability issues like hot carrier effects and electro-migration in digital circuits have a dependency on maximum power dissipation. In this article Monte-Carlo (MC) simulations have been carried out to compute and compare the reliability of the proposed design with other designs. In the MC approach, the activity of experimental data is sampled randomly so that the behavior of the circuit for the process variations can be characterized. Pseudo-random numbers are generated to converge the result gradually to an exact value. Two statistical parameters mean (µ) and standard deviation (σ) of Power, Delay,

and PDP are calculated. A higher ratio of μ and σ indicates less sensitivity of the circuit towards process variations or a higher reliability of the design. Reliability measurements of the CMOS and SG FinFET-based conventional and proposed Ring-Oscillator have been carried out along with the SG FinFET-based GLBB and LCNT-based Ring-Oscillator as shown in Table 3.

A small value of μ/σ depicts higher fluctuation in the variation of the device metric or less reliability. Reliability analysis shows μ/σ has the highest values for leakage power and PDP in the SG FinFET-based the proposed Ring-Oscillator followed by the proposed CMOS-based Ring-Oscillator. This ratio has its least value for leakage power in conventional CMOS-based Ring-Oscillator. The ratio of μ/σ for PDP in conventional CMOS-based Ring-Oscillator is a minimum which is 3.67. These figures also show that the reliability of circuits designed using FinFET technology is higher as compared to the circuits designed using CMOS technology.

The variation of performance metrics of the proposed SG FinFET-based Ring-Oscillator with the process parameters which include supply VDD, temperature, and the number of fins has been calculated. This has been done by simulating the proposed circuit at different values of VDD which range from 0.7V to 1V, the temperature which varies from 10 °C to 50 °C, and the number of fins used in SG FinFET transistors which vary from one to five.

Process variations may be a result of variation in length, width, oxide thickness, or doping concentration in the transistors. These variations change the V_{th} of the transistors which affect the leakage power, delay, and PDP of the circuit. The analysis has been carried out to verify whether the variations in the circuit parameters of the proposed circuit are stable and proper according to the theory. As the circuits are simulated at a 16nm node and a VDD of 0.7V, the chances of process variations are more. Take the example of VDD variation, the cells which are located far away from the supply voltage feel more voltage drop than other cells. Also, the noise in the voltage regulator can lead to variation in VDD. Leakage power should increase with the increase in VDD which is shown by the proposed circuit[24]. Leakage power increases with an increase in temperature in FinFET-based circuits as V_{th} decreases with an increase in temperature causing more leakage[25]. The proposed circuit exhibits this variation. The increase in the number of fins increases I_{ON} as current flows through multiple fins but also increases I_{OFF} as DIBL increases with an increase in fin width[26]. So, the effect of variation in the number of fins in the proposed circuit is also stable and proper.

Similarly, the delay of the proposed circuit decreases with an increase in VDD because the delay in FinFETs decreases with an increase in VDD. In FinFETs, the delay decreases with an increase in temperature, unlike MOSFET-based circuits where delay increases with an increase in temperature[27]. This phenomenon is called the temperature inversion effect[28]. The decrease in delay in FinFET-based circuits is attributed to the increase in tensile stress on the FinFET body which leads to band-gap narrowing and an increase in carrier mobility which increases I_{ON}, causes fast switching and decreases the delay.

An increase in delay due to an increase in the number of fins shown by the proposed circuit is due to the increases in effective width of FinFETs, which increases their gate capacitance leading to an increase in delay as well as I_{OFF}. The process parameter variations of the SG FinFET-based proposed Ring-Oscillator have been worked out and evaluated in Table 4. Similarly, the process variations of leakage power, delay, and PDP of SG FinFET-based Ring-Oscillators simulated using various leakage control techniques have been evaluated in Tables 5, 6, and 7, respectively.

Table 5 shows the leakage power variations of the Ring-Oscillators simulated using various techniques. The missing data in Tables 5, 6, and 7 are because there is no use of number of fins in CMOS based circuits hence no variation. It shows that the proposed

Table 3 — Reliability in leakage Power, Delay, and PDP of the benchmark circuit

Technique	Power (W)			Delay (ps)			PDP (aJ)		
	μ	σ	μ/σ	μ	σ	μ/σ	μ	σ	μ/σ
Conv.	89.9n	23.92n	3.76	14p	1.47p	9.52	1.25a	0.34a	3.67
GLBB	73.6u	5.89u	12.67	13.76p	0.424p	32.45	1.01f	42141f	2.4×10^{-5}
LCNT	4.62u	0.63 u	7.23	148.27p	6.16p	24.07	689.20f	120.15f	5.7
Conv (FinFET)	9.41n	0.5n	18.82	12.07p	436.11f	27.67	113.4z	2.1z	54
Proposed (CMOS)	48.19n	5.8n	8.3	164.53p	22.32p	7.37	7.8a	558.96	13.9
Proposed (FinFET)	25.59n	1.06n	24.14	259.39p	54.15p	4.79	3.98a	189.2z	21.03

Table 4 — Process parameter variation of SG FinFET-based Ring-Oscillator

Technique	VDD (V)				Temperature (°C)					Number of Fins				
	0.7	0.8	0.9	1.0	10	20	30	40	50	1	2	3	4	5
Power(pw)	47.77	80.7	132.75	168.67	23.06	36.93	62.4	108.18	188.4	47.77	95.55	143.33	191.11	238.89
Delay(ps)	67.35	42.55	28.35	23.85	97.57	86.85	71.25	65.25	57.57	67.35p	79.8p	80p	80.34p	80.89p
PDP (zJ)	3.21	3.43	3.76	4.02	2.24	3.21	4.44	7.05	10.88	3.21	7.62	11.46	15.35	19.32

Table 5 — Process Parameter variation of leakage power (W) of SG FinFET-based Ring-Oscillator

Technique	VDD (V)				Temperature (°C)					Number of Fins				
	0.7	0.8	0.9	1.0	10	20	30	40	50	1	2	3	4	5
Conv	67.55n	199.77n	610.6n	1.89 µ	55.81n	63.84n	71.77n	80.69n	90.24n	---	---	---	---	---
GLBB	34.7 µ	56.46 µ	84.05µ	117.01µ	33.14 µ	33.91 µ	34.66 µ	34.41 µ	36.14 µ	34.7 µ	69.4 µ	104.2 µ	138.9µ	173.7µ
LCNT	22.9 µ	37.46 µ	5.01 µ	75.55µ	75.46 µ	75.53 µ	75.57µ	75.6µ	75.62 µ	22.9 µ	45.83 µ	68.74 µ	91.66µ	114.57µ
Conv (FinFET)	62.22p	96.72p	146.4p	215.89p	28.16p	47.28p	82.34p	144p	253.56p	62.22p	124.44p	186.66p	248p	311.11p
Proposed (CMOS)	422.8p	657.59p	1n	19.72n	169.53p	313.85p	565.56p	990.52p	1.68n	---	---	---	---	---
Proposed (FinFET)	47.77p	80.7p	132.75p	168.67p	23.06p	36.93p	62.4p	108.18p	188.4p	47.77	95.55	143.33	191.11	238.89

Table 6 — Process parameter variation of delay (ps) of SG FinFET-based Ring-Oscillator

Technique	VDD (V)				Temperature (°C)					Number of Fins				
	0.7	0.8	0.9	1.0	10	20	30	40	50	1	2	3	4	5
Conv	13.61	10.38	8.7	7.53	11.29	11.99	12.74	13.85	14.39	---	---	---	---	---
GLBB	15.74	12.67	10.74	9.63	16.49	16.08	15.75	15.29	14.9	15.79	15.91	15.93	15.94	16.2
LCNT	111.4	45.20	24.22	17.45	18.44	17.18	17.1	16.59	15.9	111.14	119.65	130.96	134.21	138
Conv (FinFET)	11.61	9.51	8.24	7.29	12.54	12.19	11.82	11.56	11.15	11.61	11.17	11.17	12	12.21
Proposed (CMOS)	46.95	38.85	28.5	12.65	26.6	27.1	27.4	27.56	27.8	---	---	---	---	---
Proposed (FinFET)	67.35	42.55	28.35	23.85	97.57	86.85	71.25	65.25	57.57	67.35	79.8	80	80.34	80.89

Table 7 — Process parameter variation of PDP (J) of SG FinFET-based Ring-Oscillator

Technique	VDD (V)				Temperature (°C)					Number of Fins				
	0.7	0.8	0.9	1.0	10	20	30	40	50	1	2	3	4	5
Conv	919.35z	2075.68z	5312.2z	14231.7z	630.09z	761.12z	914.35z	1117.55z	1298.5z	---	---	---	---	---
GLBB	0.54f	0.71f	0.9f	1.12f	0.54f	0.51f	0.54f	0.54f	0.54f	0.54f	1.1f	1.66f	2.21f	2.76f
LCNT	2.55f	1.69f	1.33f	1.32f	1.39f	1.29f	1.29f	1.25f	1.20f	2.55f	5.48f	9f	11.7f	14.69f
Conv (FinFET)	0.722z	0.92z	1.2z	1.57z	0.35z	0.57z	0.97z	1.66z	2.83z	0.72z	1.45z	2.08z	2.9z	3.79z
Proposed (CMOS)	19.85z	25.54z	28.5z	249.45	4.51z	8.51z	15.4z	27.31z	44.7z		---	---	---	---
Proposed (FinFET)	3.21	3.43	3.76	4.02	2.24	3.21	4.44	7.05	10.88	3.21	7.62	11.46	15.35	19.32

Ring-Oscillator simulated using both CMOS and FinFET technology shows proper and stable variations of leakage power with variation in VDD, temperature, and the number of fins. It also shows the variations of leakage power with temperature are less stable in GLBB and LCNT based on Ring-oscillator compared to that of the proposed one. Table 6 gives the variation of delay of the Ring-Oscillators simulated using various techniques.

Delay in CMOS-based proposed Ring-Oscillator is increasing with increase in temperature and VDD. In the SG FinFET-based Ring-Oscillator, the delay increases with an increase in VDD and decreases with an increase in temperature due to the temperature inversion phenomenon. Table 7 gives the variation of PDP of the Ring-Oscillators simulated using various techniques. PDP of the circuits has been calculated by multiplying the instantaneous leakage power with the delay. The table 7 shows the PDP variation of the proposed circuit with VDD, temperature and the number of fins is more stable compared to other circuits.

5 Conclusions

This paper proposed a low power technique and the circuit implementations using the proposed technique. A comparative study of leakage power, delay, PDP, reliability, and the process variations offered by the circuits implemented using this proposed technique is done. The energy efficiency and robustness of circuits implemented using FinFET technology over the CMOS technology are seen. Leakage power and PDP optimization of 93.46% and 97.78% have been found in 2-input SG FinFET-based proposed NAND gate

compared to that of a 2-input SG FinFET-based conventional NAND gate. SG FinFET-based proposed 2-input NOR gate shows 98.03% and 98% optimization of leakage power and PDP, respectively compared to the SG FinFET-based conventional 2-input NOR gate. Leakage power and PDP reduction of 92.22% and 58.68%, respectively are reported in the CMOS-based proposed Ring-Oscillator compared to that conventional CMOS-based Ring-oscillator. The proposed SG FinFET-based Ring-Oscillator shows a leakage power and PDP optimization of 62.12% and 35.56%, respectively in comparison to the conventional SG FinFET-based Ring-Oscillator. From the MC analysis, μ/σ for the leakage power and PDP of SG FinFET-based Ring-Oscillator came out to be highest compared to the other Ring-Oscillators indicating the high robustness or least sensitivity of the proposed circuit towards the process variations. From the process parameter analysis carried over a 10% deviation in operating conditions, the variation in the leakage power, delay and PDP came out to stable and proper and the functionality of the proposed circuit is not affected.

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