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High resolution nuclear timing spectroscopy system based on new method of free running ramp and tracking ADCs

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The paper describes a new method for high resolution nuclear timing spectroscopy system using tracking ADCs and free running ramp to give the timing resolution of few ps over wide dynamic range of time interval extending up to few μs. The method makes use of tracking ADCs with 16 bit resolution with low conversion time of nearly 1 μs along with a free running ramp which is given as input to the two ADCs. Both the ADCs and ramp are designed to track their characteristics in order to neutralize the errors due to drift in their characteristics and hence complex system of spectrum stabilization is not required. ADC1 digitizes ramp input at the arrival of START pulse and ADC2 digitizes ramp input at the arrival of STOP pulse. The difference between digital codes of these ADCs is a measure of time interval between START and STOP pulses. New system doesn't require delay and hence biased amplifier. System has dead time of 1 μs and spectrum stabilization is easy.

Keywords: Nuclear timing spectroscopy system, Time interval measurement, Tracking ramp, ADCs

1 Introduction

Time interval measurement is required in various applications of science and technology domain, e.g., lifetime measurement in atomic energy and physics, distance measurement in laser ranging systems, time interval measurement in nuclear timing spectroscopy system[1-4]. Time interval (TI) between two signals arising from two nuclear detectors needs to be measured in conventional nuclear timing spectroscopy system, as shown in Fig. 1. Detectors produce analog pulses corresponding to incident energy of the radiation, which are further processed by Time Pick-off circuit. Time Pick-off circuit produces digital pulse at its output at the time instant which is strictly correlated with the occurrence of the input pulse. Pulses available from Time Pick-off circuits are given as START and STOP input pulses to Time-to-Amplitude-Converter (TAC). TAC produces the output voltage which is proportional to the TI between START and STOP signals. This voltage is digitized using MCA and timing spectrum is developed. For proper operation of TAC, STOP pulse is delayed using delay component which ensures that the STOP pulse will always occur after the START pulse. Because of this delay, the timing spectrum is shifted in time domain. To obtain better resolution with the limited number of channels of MCA, biased amplifier is used. The performance of conventional timing spectroscopy system is limited by efficacy of Time pick-off, TAC and MCA. To address these issues, integrated system using single ADC was proposed[5].This system doesn't make use of biased amplifier. However, the need of delay circuit still exists.

So to overcome this limitation, new system with Two Tracking ADCs is proposed in this paper.

2 New System

Free running ramp generation circuit produces periodic ramps of time period of 25.6 μs refer Fig. 2. The duration of the ramp and its frequency are governed by pulses applied to operate the analog switch. In order to obtain the stable ramp duration and its frequency, these pulses are generated using crystal controlled oscillator and counter ICs. START and STOP pulses can occur during this period, as shown in Fig. . Ramp is given as input to two tracking ADCs. At time instant T1, ADC1 receives start conversion command i.e. START pulse. ADC1 code is accessed using micro-controller ARDUINO-DUE and corresponding data is stored in the computer. Similarly at T2 time instant, ADC2 receives start conversion command i.e., STOP pulse. ADC2 code is accessed using micro-controller and stored in the computer. The difference in two digital codes is proportional to the TI. In case, when the STOP pulse arrives after START pulse, the digital code D2 will be more than D1. However when STOP pulse arrives before START pulse, the digital code D2 will be less

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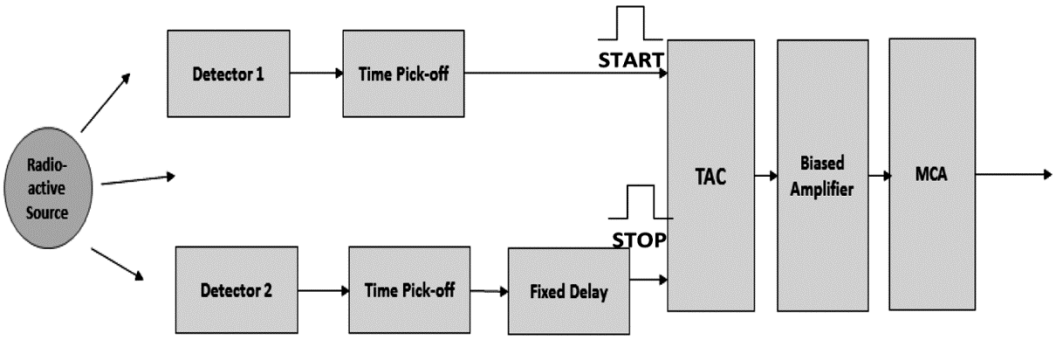

Fig. 1 — Nuclear timing spectroscopy system.

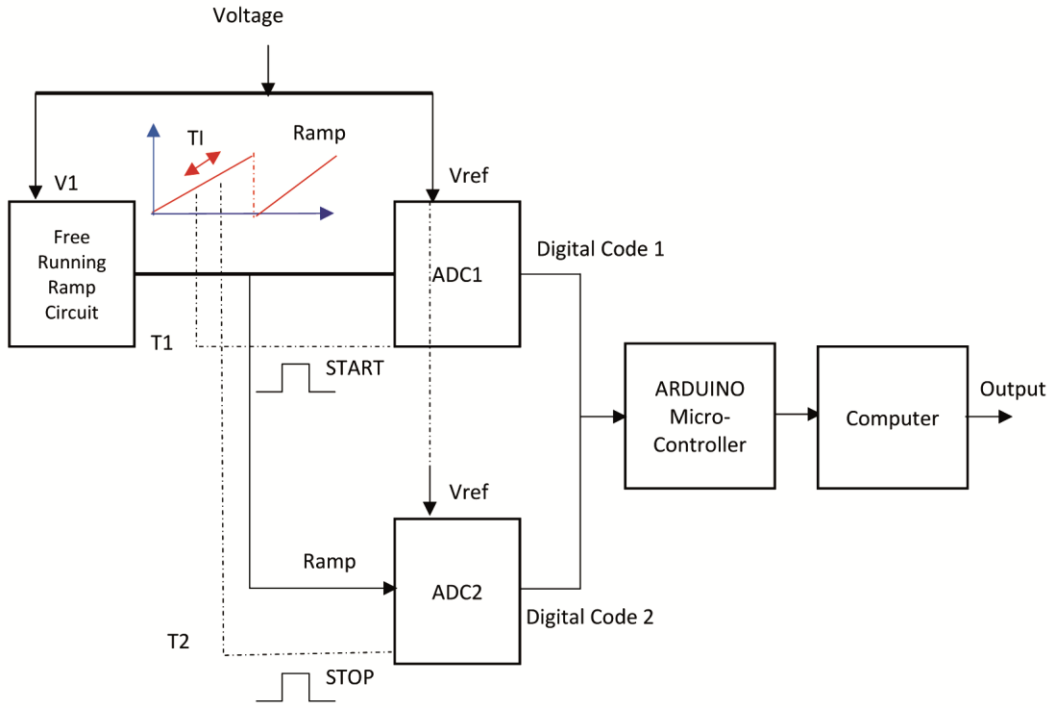

Fig. 2 — Proposed system with two tracking ADCs.

than D1. In either of these cases the difference between D1 and D2 is proportional to the TI. The events corresponding to D2 > D1 are plotted on right side of the time axis and whereas the events corresponding to D2 < D1 are plotted on left side, for timing spectroscopy applications. It is quite clear that no delay needs to be introduced after the STOP pulse similar to the one introduced in conventional timing spectroscopy systems. Hence in this case the need of additional delay and biased amplifier is totally eliminated. The behavior of the circuit is explained by mathematical equations as following.

2.1 Working of free running ramp circuit

Ramp is generated using op-amp configured as integrator, as shown in Fig. 3. The input voltage generates a current V1/R where resistor R is -R1 in series with R2. This current charges the capacitor C1 generating a linear ramp. The slope of the ramp can be adjusted by potentiometer R1.Switch is connected between op-amp inverting input and output. When switch is opened, capacitor starts charging. When switch is closed, capacitor gets discharged. This ramp output is given as input to both ADCs.

2.2 Design of integrator

Design values of Integrator:

$$Vo = \frac{Q}{C1} = \frac{1}{C1}\int i\,dt = \frac{I * T}{C1}$$

$$Let\ C1 = 4700\ pF$$

$$Vo = -5\ V$$

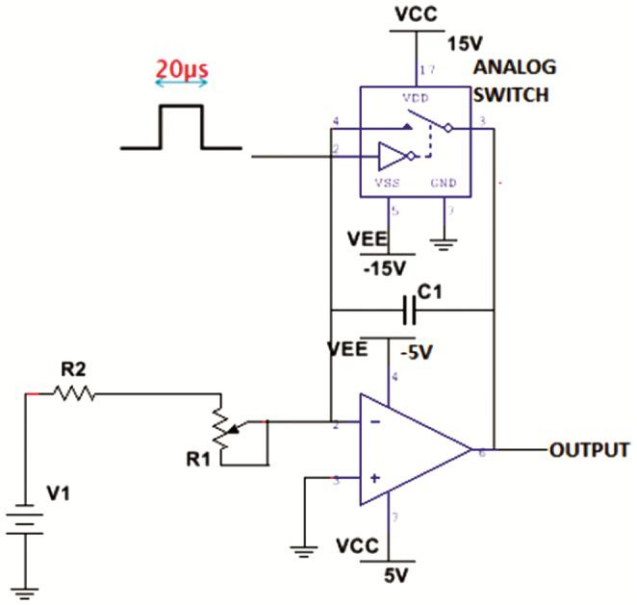

Fig. 3 — Free running ramp generation circuit.

$$I = -5 * \left(\frac{4700\ pF}{25.6\ \mu s}\right) = -917.9\ \mu A$$

$V1 = I * R\ where\ R = (R1 + R2)$ = 5V

$R = \frac{V1}{I}$ = 5.447 K-ohm

Op-amp used to generate ramp should have high slew rate, low input bias current and low input offset voltage. This ensures that ramp generated reaches to 5Vin 25.6 µs and the slope of the ramp is constant.

Refer Fig. , ramp voltage Vo1 reached in time interval T1 can be expressed as:

$$Vo1 = \frac{Q}{C1} = \frac{1}{C1}\int_0^{t1} i(t)\,dt = \frac{1}{C1}\int_0^{t1} \frac{-V1(t)dt}{R} \quad \ldots (1)$$

$$Vo1 = -\frac{T1 \times V1(S)}{RC1} \quad \ldots (2)$$

Ramp voltage Vo2 reached in time interval T2 can be expressed as:

$$Vo2 = \frac{Q}{C1} = \frac{1}{C1}\int_0^{t2} i(t)\,dt = \frac{1}{C1}\int_0^{t2} \frac{-V1(t)}{R}\,dt \quad \ldots (3)$$

$$Vo2 = -\frac{T2 \times V1(S)}{RC1} \quad \ldots (4)$$

Ramp voltages Vo1 and Vo2 are digitized by ADC, hence Vo1 and Vo2 can be expressed as:

$$Vo1 = \frac{V_{ref}}{2^N}\,D1 \quad \ldots (5)$$

V_{ref} is the reference voltage connected to ADC and D is the decimal equivalent of binary code produced by ADC, hence

$$D1 = \frac{Vo1 \times 2^N}{V_{ref}} \quad \ldots (6)$$

$$D2 = \frac{Vo2 \times 2^N}{V_{ref}} \quad \ldots (7)$$

TI can be expressed as following:

$$T2 - T1 = (Vo2 - Vo1)\frac{RC1}{V1} \quad \ldots (8)$$

$$T2 - T1 = \left\{\left(\frac{D2 \times V_{ref}}{2^N}\right) - \left(\frac{D1 \times V_{ref}}{2^N}\right)\right\}\frac{RC1}{V1} \quad \ldots (9)$$

$$T2 - T1 = (D2 - D1)\left(\frac{V_{ref}}{2^N}\right)\frac{RC1}{V1} \quad \ldots (10)$$

If Vref and V1 are the same, then the above equation be simplified as:

$$T2 - T1 = (D2 - D1)\left(\frac{RC1}{2^N}\right) \quad \ldots (11)$$

From above equations it is clear that when Vref is equal to V1, the TI is governed by only (D1-D2) and RC1 and independent of any value of reference voltage. Referring to above equation, it is clear that

TI measurement is independent of V1 and Vref fluctuations and hence ramp slope variations. Conventional timing spectroscopy system, TAC and MCA are separate components and hence TAC performance is affected by ramp slope variations because of V1 fluctuations.

Slope variations because of resistor-R and capacitor-C1 can be minimized by using metal film resistors and deep mica capacitors.

Therefore spectrum stabilization is easy for proposed integrated timing spectroscopy system.

2.3 Advantages of proposed scheme

(i) Since delay is not required for system implementation, system doesn't have errors contributed by delay component. Moreover the resolution of the system is not affected by delay component accuracy and jitter. 16 bit ADC is proposed for this system. So with 25.6 µs ramp, almost 390 ps resolution can be obtained. For obtaining better resolution of 100 ps, the time duration of ramp can be reduced suitably. The system has been tested for ramp duration of 3.5 µs wherein the resolution of 106 ps is obtained.

(ii) Wider range of 25 µs obtained compared to the conventional timing spectroscopy systems.

(iii) Biased amplifier is not required, since delay is not used in the system. System design has eliminated the requirement of delay and biased

amplifiers for implementation of timing spectroscopy system.

(iv) Dead time of the conventional timing spectroscopy system is in the range of 10 micro-sec. Proposed system here makes use of ADC – AD7980 which has conversion time of 1 µs. Further ADC output digital code can be saved on board memory and then can be accessed by micro-controller. So dead time of proposed system is of the order of 1 µs. This is major achievement over conventional systems.

(v) Proposed system makes use of free running ramp. Hence the nonlinearities encountered near the START region of the ramp in the conventional system are totally removed.

(vi) Further the ramp generation and ADCs are made to track over the entire temperature range because of which the spectrum stabilization is easy.

(vii) Time interval measurement range and resolution can be adjusted by changing ramp duration from few hundreds of ns to few tens of µs.

(viii) Non linearities in the channels of ADCs are compensated because of occurrence of time interval on various sections of free running ramp. Additional linearization technique is not required in the designed system.

3 Performance of System

Performance of the designed system is obtained and presented in Fig. 4.

3.1 Experiment 1 – To test linearity of the ramp

Ramp is given as input to two ADCs and START pulse is generated using comparator. For generating START pulses on various portions of the ramp, the ramp is given as one input to the comparator and other input is a DC threshold voltage which is varied using the potentiometer. START pulse acts as start of conversion (SOC) pulse for ADC1. Further comparator output is connected to Programmable Timing Element (PDG). PDG code is configured to give 1 µs delay at the output. This PDG delayed output pulse acts as STOP pulse. STOP pulse is used as SOC pulse for ADC2. ADCs code is obtained using arduinomicro-controllers. Using PDG pulse as STOP pulse, ensures that the comparator jitter appears in START as well as STOP pulse. Non-linearity of the ramp is tested by shifting TI event on different sections of the ramp. Refer Fig. 5, ADC1 and ADC2 average count is observed to be varying linearly with the variation in comparator output. Also the offset observed between two ADCs average count is almost constant throughout the experiment. The characteristics in the graph which are parallel to the X-axis are due to the constant threshold set by the potentiometer whereas the characteristics which indicate slopes are during the process of variation of the threshold. During the entire process, START and STOP pulses are continuously received by both ADCs.

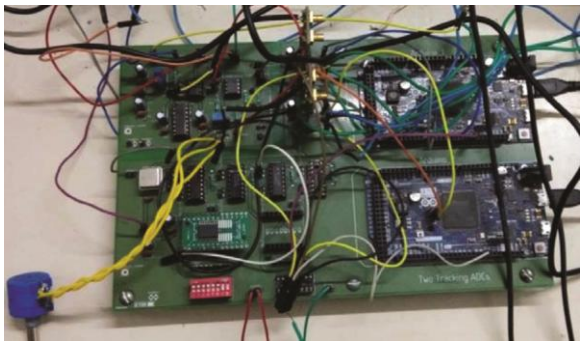

Fig. 4 — Actual system of two tracking ADCs.

3.2 Experiment 2 – To measure ADC code variation for input noise and jitter

Two tracking ADCs are provided with same DC input and SOC for ADCs is generated using clock. Refer Fig. 6, offset variation between two ADCs count is observed. It is observed that ADC code variation due to noise for the same DC input connected to both the ADCs is nearly +- 2 LSBs for 16 bit resolution.

3.3 Experiment 3 – To measure TI resolution of system

Ramp is connected to two ADCs and SOC pulse is obtained using comparator. This SOC is connected to two ADCs. ADCs code offset variation is observed,

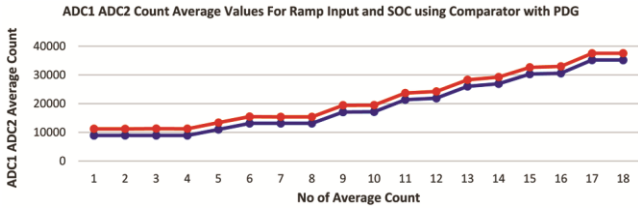

Fig. 5 — Performance of two tracking ADCs system for ramp linearity.

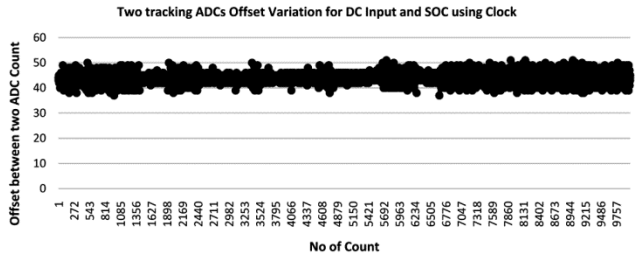

Fig. 6 — Performance of two tracking ADCs system for DC input.

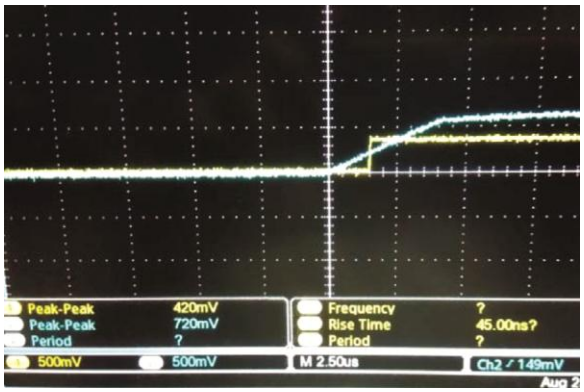

Fig. 7 —Two tracking ADCs offset variation for ramp input and SOC using comparator.

refer Fig. 8. Further comparator threshold voltage is varied and the experiment is performed. Ramp reaches to 5v in 3.5 µs, refer Fig. 7. With 16 bit ADC, the best resolution for TI measurement is

3.5 µs/65536 = 53 ps.

Referring Fig. 8, the offset variation is seen to be +- 2 counts about the offset average value. This shows that the offset variation for ramp input is of the order of 53 ps * 2 = 106 ps. Hence TI of the order 100 ps can be precisely measured using this system.

Further, for the given input time interval TI measurement, depending upon START and STOP pulse arrival, i.e. if START pulse comes before STOP pulse, time interval TI is obtained by subtracting ADC2 code from ADC1 code (D2-D1). If STOP pulse comes before START pulse, then time interval TI is equal to ADC1 code minus ADC2 code (D1-D2). In these measurements, two individual ADC code values can differ by +- 0.5 LSB. Assuming extreme conditions, i.e. ADC1 code varies by +0.5 LSB and ADC2 code varies by -0.5 LSB, then the maximum error or spread in TI measurement would be 1 LSB. Experiment 3 is conducted to measure this spread in the ADC code by providing same SOC to the two ADCs for the given ramp instant at the input. Experiment shows that the maximum spread in TI measurement can be LSB * 2

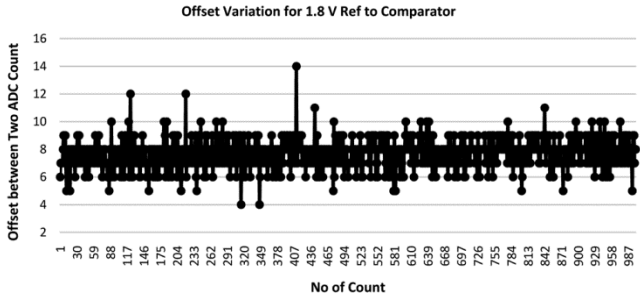

Fig. 8 — Two tracking ADCs offset variation for ramp input and SOC using comparator.

counts, which includes all the errors and factors for the TI spread in the measurement system.

Hence the resolution offered by the system for TI measurement is of the order of 100 ps for a ramp duration of 3.5 µs. Further the spread can be reduced to 1.5 ps by using ramp duration of 100 ns.

4 Conclusions

In this work, integrated system for timing spectroscopy system has been proposed, designed and tested for the capabilities of precise TI measurement. Using this system it was possible to measure TI with resolution of 106 ps, as demonstrated in Fig. 8. Initially ramp linearity is tested as shown in Fig. 5. Further ADC code variation due to noise has been observed for the same DC input connected to both the ADCs, which is nearly +- 2 LSBs for 16 bit resolution, as shown in Fig. 6. The proposed integrated system capability is tested with ramp time period of 3.5 µs to 25.6 µs offering resolution of nearly 106 ps to 390 ps respectively. It should be possible to improve the resolution to less than 10 ps by proper PCB Layout to reduce the effect of noise.

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