Indian Journal of Pure & Applied Physics
Vol. 59, March 2021, pp. 163-167

Nullor Based New Implementation of CDBA Using Current Feedback Operational Amplifier

Bhawna Aggarwal*, Shubaangi Bisht, Shreya Gupta, Vidushi Goel & Shweta Gautam

Electronics and communication Engineering Division, Netaji Subhas University of Technology, New Delhi-110 078, India

Received 27 January 2021; accepted 17 February 2021

In this paper, a methodology based on nullors and passive elements to create equivalent circuits for existing building blocks has been presented. This methodology has been used for generating the equivalent nullor circuit for Current Differencing Buffered Amplifier (CDBA) and its implementation through AD844 ICs of Current Feedback Operational Amplifier (CFOA) has been presented. The proposed circuit is further modified by replacing the equivalent nullor sections with smaller blocks. The implemented CDBA (proposed CDBA-I) has been simulated and compared with existing topologies of CDBA to represent its proper functioning using LTSPICE. The proposed CDBA configuration offers a symmetric structure for its 2 differential inputs and offers higher bandwidth. Moreover, the configuration has been modified further to achieve low noise output terminal by the use of another CFOA (proposed CDBA-II). Both of these proposed configurations have been simulated and verified experimentally.

Keywords: Nullator, Norator, Nullor, Current Differencing Buffered Amplifier, Current feedback operational amplifier.

1 Introduction

Nullor is a pathological element that is composed of a ‘nullator’ and a ‘norator’ and was first introduced by Carlin in 1964 (Ref. 1). Nullors provide the advantage of being universal building blocks. Almost all existing analog circuits like Negative Impedance Converter (NIC), gyrator, unilateral voltage amplifier, all types of controlled sources can be represented using nullors and resistors, alone[2,3]. The nullor concept has been extended for the design and analysis of a variety of circuits such as filters, sinusoidal oscillators and immitance networks[4,6,7]. In literature various synthesis methods for realizing pathological representation of existing circuits have been proposed. However, these methods are complex and involve time consuming matrix operations for complete synthesis. This paper presents an alternate methodology based on nullors and passive elements to create equivalent circuits for existing building blocks using ICs that are commercially available. The presented methodology has been verified by generating the equivalent nullor circuit for Current Differencing Buffered Amplifier (CDBA) and its implementation through AD844 ICs of Current Feedback Operational Amplifier (CFOA) has been presented. This methodology is not limited to a particular circuit or a specific building block. It is a generalized technique and can be used to generate multiple realizations for a circuit.

Theoretical analysis regarding functional blocks like nullors, CFOA and CDBA is provided in section 2. The nullor based methodology used to create equivalent circuits for existing building blocks has been detailed in section 3, along with the proposed implementation of CDBA. Section 4 summarizes the simulation results followed by experimental results in section 5. Finally, conclusion section concludes the paper.

*Corresponding author (E-mail: kbhawnagarg@yahoo.co.in)

2 Functional Blocks

2.1 Nullor

A nullor represents an ideal amplifier, possessing infinite current, voltage, transconductance and transimpedance gains[1]. It is a theoretical two-port network consisting of a nullator at its input and a norator at its output terminals. Nullator and norator are pathological two-terminal elements that are described by their terminal behavior. A nullator is defined as a device which possesses zero current as well as zero voltage. However, terminal current and terminal voltage of a norator is arbitrary and can independently take on any value. In literature, equivalent nullor representation of BJTs, FETs, current conveyors (CC), operational transconductance amplifier (OTA) and opamps have been formulated[8,9]. Subsequently, nullors have been used to generate equivalent models of a large number of different active blocks.

2.2 Current feedback operational amplifier

Current feedback operational amplifier (CFOA) is a 4-terminal current mode, active device. It consists of second generation current conveyor (CCII+) followed by a voltage buffer. The behavior of a CFOA in terms of its input terminals (X and Y) and output terminals (W and Z) is defined as:

$$i_y = 0;\ v_x = v_y;\ i_z = i_x \ and\ v_w = v_z \quad \ldots (1)$$

CFOA offers very high slew rate and is free from gain-bandwidth product limitations. Moreover, CFOAs are commercially available in the form of 8-pin AD844 ICs. Due to its current feedback architecture it has better AC performance, linearity and pulse response[10].

2.3 Current Differencing Buffered Amplifier

Current Differencing Buffered Amplifier (CDBA) is a 4 terminal transimpedance amplifier. The matrix equation representing current-voltage relationship of CDBA for its input terminals (p and n) and output terminals (W and Z) is given as:

$$\begin{pmatrix} i_z \\ v_w \\ v_p \\ v_n \end{pmatrix} = \begin{pmatrix} 0 & 0 & 1 & -1 \\ 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{pmatrix} \begin{pmatrix} v_z \\ i_w \\ i_p \\ i_n \end{pmatrix} \quad \ldots (2)$$

It is free from constant gain-bandwidth product limitations and can be operated in both current and voltage modes[9]. It has been extensively used in the realization of MOSFET-C filters, current mode multipurpose filters for analog signal processing, impedance converters, impedance inverters and polyphase filters[11]. In literature, implementation of CDBA using two CFOAs was proposed by Acar and Ozoguz in 1999 in[12]. Koksal et al. in 2009 proposed a new design with 3 CFOAs[13] that reduces the noise of W-terminal. However, both of these CDBA circuits are not balanced and show different behavior when signal is applied at p terminal or n terminal.

3 Implementation of CDBA using nullor equivalence

The circuit implementation methodology discussed in this paper is based on the fact that, if the equations describing voltage and current behavior of the circuit are given, its symbolic representation can be derived directly from the mathematical equations, without performing any operations. A step-by-step procedure for implementation of CDBA is given as: Firstly, nullor equivalence model of CDBA is generated. This equivalence model has to be designed by observing current and voltage behavior of CDBA and comparing it with that of nullor characteristics. This nullor equivalence model of CDBA is shown in Fig. 1.

Secondly, the designed model is compared with nullor models of standard blocks. It has been inferred that the red encircled section of CDBA can be realized by a CFOA and the blue encircled part (shown by dashed line) can be realized using CCII-. Since CFOA has been selected as the basic building block, CCII- is further implemented using two CFOAs. Thus, a total of 3 CFOAs are required for the complete representation. The proposed circuit of CDBA (proposed CDBA-I) designed using this methodology is shown in Fig. 2 (shown in bold rectangular box).

The X terminals of AD844-1 and AD844-2 represent the p and n terminals respectively of CDBA. Along with this, W and Z terminals of AD844-3 form respectively W and Z terminals for the realized CDBA. In this proposed structure of CDBA, p and n terminals are

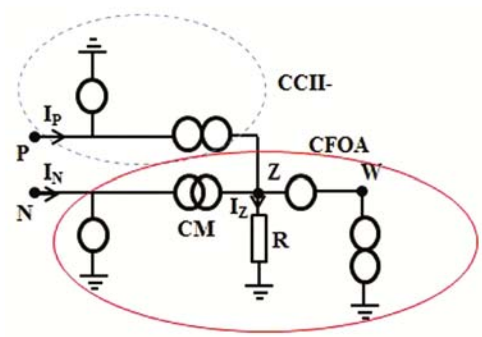

Fig. 1 — Nullor representation of CFOA

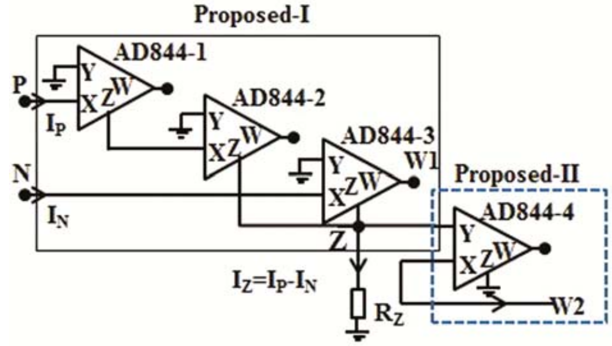

Fig. 2 — (a) 3 CFOA based proposed CDBA-I (b) 4 CFOA based proposed CDBA-II.

symmetrical and balanced. This configuration gives the flexibility of applying the signal at either of p or n terminals with equal efficacy. However, in proposed CDBA-I, the noise characteristics of W terminal is equivalent to CDBA structure given in Ref. 12. To avoid this noise, proposed CDBA-I can be modified by adding an additional AD844. This modified implementation of CDBA (proposed CDBA-II) is shown in Fig. 2. In proposed CDBA-II, p, n and Z terminals are same as that of proposed CDBA-I. However, W-terminal has been implemented by the X terminal of AD844-4 and has been denoted as W2 in Fig. 2. The proposed CDBA-II provides symmetrical p and n terminals, along with noise free W terminal. However, the implementation of proposed CDBA-II requires an additional AD844.

4 Simulation Results

All the 4 topologies of CDBA, discussed in the paper ((Ref. 12), (Ref. 12) and proposed ones) have been implemented in LTSPICE using standard model of AD844. These different structures of CDBA have been analyzed and their various comparative results have been presented in this section. To obtain comparison in different parameters their dc, ac and transient analysis have been carried out. For all these analyses a resistance of 100Ω is connected at Z terminal of CDBA.

4.1 DC analysis

DC analysis has been carried out by varying the applied input current from -10mA to +10mA. Variation of output current at Z terminal with respect to differential input voltage (Ip-In) for proposed CDBA-I and CDBA-II have been represented in Fig. 3(a). For these CDBAs, the respective variations in output voltage (Vw) have been plotted in Fig. 3(b). These figures show that output current and voltage completely follows the variations in input differential current. The % error in output current at Z terminal, for conventional and proposed CDBAs has observed in LTSPICE. It has been analyzed that all the configurations provide current at Z terminal with very high accuracy, % error being lower than 0.04% in the complete range. The error being minimum in conventional 2 CFOA based CDBA and proposed-II CDBA. The % error in output voltage at W terminal is minimal for conventional 2 CFOA based CDBA and proposed CDBA-I.

4.2 AC analysis

AC analysis for the CDBAs discussed in the paper have been carried out for a frequency range from 100Hz to 500 MHz. Fig. 4(a) shows the frequency response for these CDBAs, output being observed at Y terminal. From this response, it can be seen that the bandwidth looking from Z terminal is 877.65MHz for conventional CDBAs and 949.13MHz for proposed CDBAs. However, this is obtained with ringing effect in the proposed structures. The frequency response observed for the CDBAs for output taken at W terminal is shown in Fig. 4(b). This figure shows a

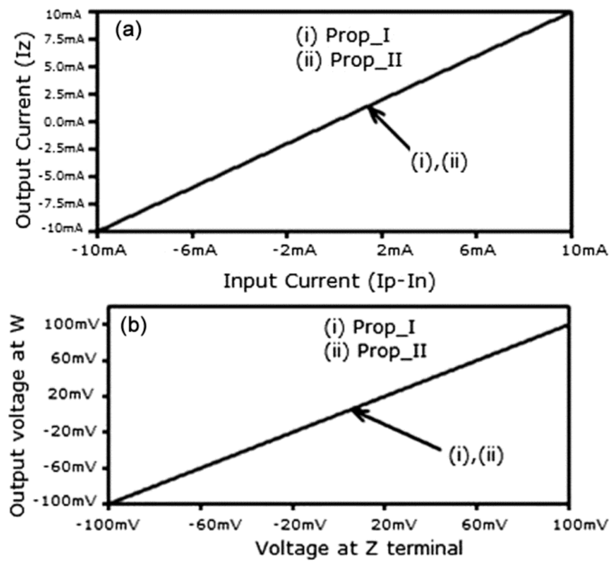

Fig. 3 — Variation of (a) output current (Iz) (b) output voltage (Vw) with respect to voltage at Z terminal due to variations in differential input current (Ip-In)

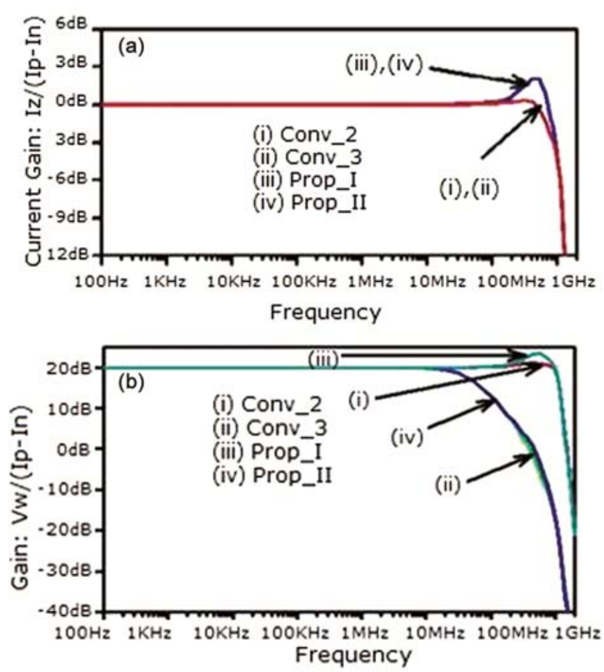

Fig. 4 — Frequency response representing gain and bandwidth at (a) Z terminal (b) W terminal

Table 1 — Comparative simulation results summary for the 4 CDBA configurations

Parameter			Conventional 2 CFOA based CDBA (Ref. 12)	Conventional 3 CFOA based CDBA (Ref. 13)	Proposed CDBA-I	Proposed CDBA-II
No. of CFOA used			2	3	3	4
Max. % error	Iz		0.002	0.03	0.04	0.01
	Vw		0.013	1.19	0.012	1.19
Bandwidth (MHz)	Z terminal		877.65	877.65	949.13	949.13
	W terminal		1100	49.36	1100	49.9
R_{in} (Ω)	p terminal		36	36	36	36
	n terminal		50.12	50.12	36	36
R_{out}	Z terminal (MΩ)		2.99	4.1	1.5	1.73
	W terminal (Ω)		15	50	15	50
Slew rate (V/µs)	Z terminal	Rising Edge	1704	1665	909	911
		Falling Edge	1513	1640	903	909
		Average	1608.5	1652.5	906	910
	W terminal	Rising Edge	1474	1670	870	923
		Falling Edge	1400	1578	835	899
		Average	1437	1624	852.5	911
Input referred noise	Z terminal (pA/Hz½)		41.52	41.52	41.92	41.92
	W terminal (nA/Hz½)		18.21	4.98	18.21	4.98

slight increase in bandwidth of proposed-II CDBA. The input resistance (R_{in}) and output resistance (R_{out}) for various CDBAs have been examined from their p and n terminals. It has been observed that R_{in} for proposed CDBAs is exactly same looking either from p or n terminal and is equal to 36Ω. However, R_{in} for conventional CDBAs changes to approximately 50Ω, when being observed through n terminal. Thereby, reflecting the symmetric nature of proposed CDBAs. All these simulated values have been summarized in Table 1.

4.3 Transient and noise analysis

Transient analysis has been performed to calculate slew rate for the CDBAs. For this a pulse signal of ±10mA amplitude and 10MHz bandwidth has been applied at the input terminal. The response obtained has been shown in Fig. 5 (a) and (b) for output voltage observed at Z and W terminals respectively. These figures show a decrease in slew rate of the proposed CDBAs. Noise analysis has been carried out for all the 4 CDBA configurations. This analysis showed that proposed-II CDBA offers less noisy W terminal as that of conventional 3 CFOA based CDBA. However, the noise at Z terminal is equivalent in all 4 configurations. All these simulation results and those mentioned above for various CDBAs have been summarized in Table 1.

From these simulation results, it is observed that symmetric CDBA structures for n and p input terminals can be obtained, while maintaining the low noise figures for Z and W terminals with the help of proposed CDBA designs. They also offer increment in bandwidth at Z terminal. However, their implementation requires an additional CFOA and they offer lower slew rate.

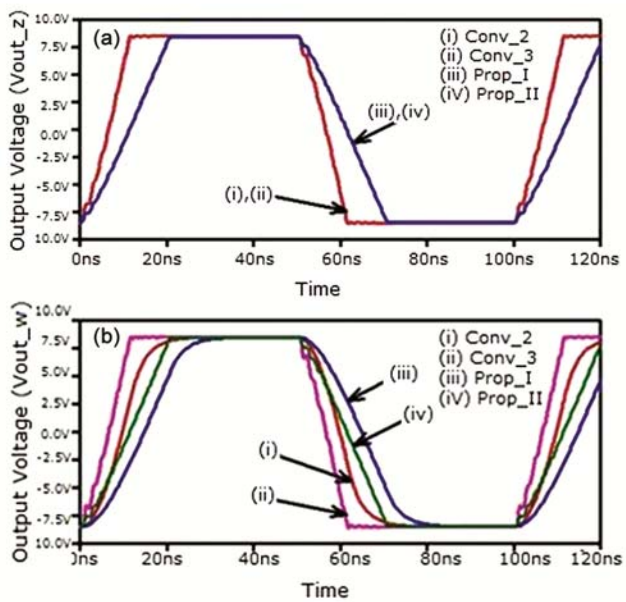

Fig. 5 — Output voltage response for step input signal as observed from (a) Z terminal (b) W terminal

5 Experimental Results

To practically verify the working of proposed CDBA circuits, they have been implemented on bread board using AD844 ICs. Input current (Ip/In) has been provided by connecting respective terminals to variable voltage source (Vp/Vn) through a 3.3KΩ resistor. This arrangement works well as in this circuit, Ip and In terminals are at virtual ground. Required variations in currents are obtained by varying these voltages. ICs of AD-844 used in the experiment have been biased with supply voltage of ±10V. It has been observed that Iz follows (Ip-In) and Vw follows Vz upto 10MHz frequency. After which the voltage Vw starts falling. These results justify the operation and usability of the proposed CDBA configurations in practical environment.

6 Conclusion

In this paper, a new methodology for realizing circuits based on their equivalence with Nullor model has been proposed. A new configuration for CDBA (proposed-I CDBA) has been realized by this method. CDBA has been chosen as basic block due to its versatility and flexibility to be used both as current mode and voltage mode device. This proposed configuration of CDBA offers near ideal characteristics with the advantage that its 2 input terminals are symmetrical. Moreover, the configuration has been further modified to obtain low noise output W terminal. These proposed circuits have been verified and compared with conventional circuits using LTSPICE. These results show that the proposed circuits provide symmetrical inputs and higher bandwidth, while maintaining low noise characteristics of the conventional CDBAs. Further these circuits have been practically implemented on bread board using AD844 ICs and verified for their usability in practical environment.

References

1 Carlin H J, *IEEE Trans Circuits Theory*, 11 (1964) 67.
2 Carlin H J & Youla D C, *Proc IRE*, 49 (1961) 907.
3 Kumar P & Senani R, *Anal Integr Circuits Signal Process*, 33 (2002) 65.
4 Bruton L T & Pederson R T, *IEEE Trans Circuits Theory*, 20 (1973) 294.
5 Liu S I & Liao Y H, *Int J Electron*, 81 (1996) 171.
6 Hou C L, Wang W Y, *Microelectron J*, 29 (1998) 59.
7 Senani R, *IEEE Trans Circuits Syst*, 33 (1986) 323.
8 Sanchez-Lopez C, Fernandez F V, Tlelo-Cuautle E & Tan S X, *IEEE Trans Circuits Syst I: Reg Papers*, 58 (2011) 1382.
9 Myers B R & Martinelli G, *Proc IEEE*, 53 (1965) 758.
10 Senani R, Bhaskar D, Singh A & Singh V, Current feedback operational amplifiers and their applications, Springer, New York, (2013) 25.
11 Sağbaş M, *Turk J Electr Eng Comp Sci*, 19 (2011) 565.
12 Acar C & Ozoguz S, *Microelectron J*, 30 (1999) 157.
13 Koksal M, Oner S E & Sagbas M, A New Second-Order Multi-Mode Multi-Funtion Filter Using a Single CDBA, Antalya, Turkey, *Eur Conf Circuits Theory Des Conf Prog*, (2009) 699.