adder trees and partial product generators.[5] The proposed architecture is an area efficient DA based FIR filter, which saves 80% of the slice logic compared with the conventional DA and decomposed DA methods. Step Limiting Bull-Horrocks Modified (SLBHM) and Step Limiting n-dimensional Reduced Adder Graph (SLRAGn) algorithms have been proposed with the least number of adders steps in order to implement the FIR filters.[6] They contrasted the results with the existing algorithms and shown that the required number of adders steps are less at lower values of the order. The proposed algorithms are not giving optimized results in terms of adder steps as the order of the filter is increasing. But the tradeoff between area and speed is effective even for higher values of the order of the filter. The area efficient and fast multiplier techniques are presented, these multipliers are suited for the filtering operations as they are giving less computation time with less hardware utilization.[7,8]

The FIR filter with LUT cascaded based implementation using weighted-sum (WS) functional decomposition has been proposed.[9] For serial multiplication of coefficients and delayed input sample signals requires more hardware functional blocks and takes more time to compute the result. To avoid the shortcomings of the serial multiplication the authors proposed parallel multiplication with the help of cascaded LUT. The implementation requires less number of LUTs and memory, when compared to the RAM based implementation. The FIR filters with intellectual property cores has been proposed with data path and controller block.[10,11] Where coefficients are supplied from the controller block and data samples are getting from datapath unit. For each selection of bandwidth the user has to give the control information, therefore utilizing these core structures in the real time applications will be difficult. The parameterization of datapath for order 2, 4, 6, and 8 has taken and presented the results with 33% & 48% less power utilization and 10% increase in the area utilization.

An MCM direct form Block FIR filter with lesser power and greater speed utilization implementation was presented.[12] The entire function is divided into several blocks and each block will be executed parallel to increase the speed of the operation. A 5 way 6 tap filter presented by the authors, requires more area due to additional circuits like Serial In Parallel Out (SIPO) and Parallel In Serial Out (PISO) at the input and output of the filter respectively. The block FIR filter is suitable for fixed set coefficients and less number of taps. If the filter order increases, it increases the overhead of additional circuits like SIPO and PISO, which in turn increases the overall area of the filter.

The high speed and low complexity multipliers have been proposed with the canonical signed digit (CSD) coefficients.[13] Pipelined Registers are inserted within multiplier's critical path to reduce the overall delay, thereby increasing the speed of computations. The length of the critical path is estimated to decrease around 33% of the existing critical path without pipeline registers. It indicates the pipelined registers would consume the logic overhead, which increase the utilization of the silicon area during the full custom implementation of the design.

The low complexity reconfigurable digital bandwidth filters are proposed with cascading of subband filters.[14,15] These reconfigurable digital filters can be tunable over audio frequency range. The coefficients are represented by CSD format. Using Farrow structure and CSD coefficients, the single bandwidth filters are used to generate variable bandwidth. The values of the coefficients are slightly adjusted to get the new bandwidth of the filter. The authors proposed a low complexity variable bandwidth filter with multiplier less architecture. The proposed implementation is simulated for digital hearing aid requirements. The reduction of hardware complexity of the FIR filters with the help of CSD representation has been discussed.[16] The authors also mentioned the errors involved due to the non zero CSD coefficients. Due to increase of the non zero CSD coefficients, the value of the error is prone in the stopband extrema. In order to reduce the errors in the stopband the minimum non zero CSD reductions should be 3 non zero digits and it gives an optimal solution.

For semicustom implementation of reconfigurable filters requires the target device. There are several semicustom ICs available with large amount of logic utilization and network interconnect resources, such as FPGAs. The crossbar architectures with 16 bit granularity is suitable for the DSP applications.[17] The central crossbar and multiple crossbar fabrics are used in the crossbar architectures with routing mappings, these fabrics and mappings allow the user to implement the reconfigurable architectures in the semicostum implementation. The internal architecture

representation of digital signals. Multiple pass bands can be achieved with the help of clock gating technique. The Phase detector circuit should give its decision and depending upon the reference signal's value and the input clock signal. The phase detector is used to compare the reference clock signal with the input clock signal and the decision is made based on the values of both signals. For more pass bands, it requires to generate multiple reference signals. The width of phase detector output depends on the number of pass bands required. Control logic will select one set of coefficients stored in the LUTs. For each specific pass band, there will be a set of coefficients. State machine inside the control logic selects any one set of coefficients based on the decision made by phase detector circuit.

Simulation Results

Reconfigurable FIR filter with control logic with 11 taps and 16 bits has been simulated in a Xilinx ISIM simulator with Virtex4 XC4VFX12 device as a target device. The simulation results are compared with UDF and FDF reusable SoC designs.

The coefficients generated using MATLAB R2021a are listed in Table 2. These two sets of coefficients are stored in the control unit and one of the sets will be supplied to the FIR filter automatically based on the value of the clock signal. The schematic diagram generated after synthesizing with RTL schematic is shown in the Fig. 4. The device utilization of the implementation is verified after synthesizing the multiband reconfigurable FIR filter. The number of slices utilized out of the total resources available in the virtex 4 device is only 1%. Similarly the remaining resources utilized like BUFG, DSP48s and external IOBs are observed to be 6%, 34% and 17% of the available resources as shown in Table 3. The devices like one 16 × 7 to 22 MAC unit, nine 16 × 7 multipliers, nine 16 × 7 adders and registers utilized in the implementation are listed in the Table 4. The sizes of the MAC, multipliers and adders will vary based on the bit width of the input signal and coefficients.

The simulation results shown in the Fig. 3 is the multiband reconfigurable FIR filter with 16 bits and 11 taps was implemented with the same architecture of the MAC based filter design. The area utilization comparision is always made based on the number of LUTs occupied in the design from the existing methods. Here it is observed from the comparison

Fig. 6 — magnitude and phase response of ω_{p3} = 0.55π to ω_{p4} =0.70π

Table 2 — Coefficients for selected bandwidths

Coefficient	h0	h1	h2	h3	h4	h5	h6	h7	h8	h9	ha	hb
First Set	0	−2	−6	−5	7	21	21	7	−5	−6	−2	0
Second Set	0	−2	6	3	−18	12	12	−18	3	6	−2	0

Table 3 — Device Utiliation Summary

Name of the Device	Resource utilization out of Available resources	% utilization
Number of BUFGs	2 out of 32	6%
Number of DSP48s	11 out of 32	34%
Number of External IOBs	41 out of 240	17%
Number of Slices	82 out of 5472	1%
Number of SLICEMs	0 out of 2736	0%
Number of LOCed IOBs	0 out of 41	0%

Table 4 — Advanced HDL Macro Statistics

Device	Number of Units for Filter with Order(n) 11
16×7-to-22-bit MAC	1
16×7-bit multiplier	9
16×7-bit registered multiplier	1
16-bit adder	9
Flip-Flops	133
1-bit latch	1
6-bit latch	10

Table 5, that there are a very few number of 4 input LUTs utilized for the proposed implementation. It is observed that the proposed implementation requires 79.8% less number of 4 input LUTs than the existing UDF architecture and 83.3% less number of LUTs than FDF architecture. The UDF and FDF are the methods used in the design of reconfigurable FIR filter design for multiple pass band. The number of

Table 5 — Comparison Table

Parameter	UDF 16bit 11 taps[1]	FDF 16bit 11 taps[1]	Proposed RFIR 16bit 11 taps
Slice Register	405	420	137
Flip Flop	85	132	133
Latches	320	288	4
4 input LUTs	752	913	152

Table 6 — Operating Frequency & Timing Report

Parameter	Filter with order(n) 4	Filter with Order(n) 11
Min. time period	1.353ns	1.353ns
Max. operating frequency	738.962MHz	738.962MHz
Min. I/P arrival time before clock	5.606ns	15.269ns
Max. O/P required time after clock	4.997ns	5.405ns

slice registers for the proposed implementation would utilize around 33% of both the existing architectures. The operating frequency and timing responses are presented in the Table 6.

Conclusions

The implementation of reconfigurable FIR filter using control logic is proposed in the paper, which is suitable for allowing multiple band of frequencies with the help of single FIR filter and multiple set of coefficients. The implemented design requires less amount of silicon space when compared to the existing architectures for multiple passband filters. The automatic selection of coefficients has been used to get multiple band of frequencies. The high data rates, area efficiency and multiple passband filters are the key factors for 5G communications. The area efficient reconfigurable FIR filter has been implemented with MAC based FIR architecture. The simulation result of the proposed architecture shows that, it can save 79.8% to 83.3% of the 4 input LUTs and requires only 33% slice registers compared to the existing UDF and FDF FIR filter architectures. The total power consumed by the device is 177.7 mW and static power consumed is around 166.6 mW. The implemented device can be operated at a maximum frequency of 738 MHz.

The speed of the filters can be further improved by incorporating the LUT based designs to avoid the multiplication operations. For the design of linear multiple passband FIR filters, the coefficients are similar over center coefficient. Therefore to reduce the overall area of the multiplier and to improve the speed of multiplications, folded structures can be used.

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