Journal of Scientific & Industrial Research
Vol. 82, January 2023, pp. 86-92
DOI: 10.56042/jsir.v82i1.70256

Sustainable and Short-range Communication Techniques for Smart Industry Environment

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Received 08 May 2022; revised 02 October 2022; accepted 07 October 2022

The industries of the future, call for unprecedented flexibility whereas, the communication technology intervention is the best solution. For sustainable development goals in industry automation demand Dedicated Short-range Communication (DSRC) with Intelligent Transportation Systems (ITS). One of these systems' view point is the regular dissemination of safety messages. Integrating this technology with the existing Industry automation is a technical challenge. Integration also involves in imparting intelligence through digitalization of communication. With a cost of overhead power, Error Controlling Codes (ECC) provides a reliable and error-free DSRC communication system. In this paper, low power and secure digital VLSI architecture is presented to meet the sustainable integrated communication technology on chip circuitry for industry 4.0. The circuit's performance is measured in Cadence utilizing 18 nm FinFET-based ECRL adiabatic logic. The design provides maximum power savings of 99.49% over reported values for CMOS and 99.41% for pass transistor implementation. The adiabatic logic circuits constructed with ECRL are shown to have consistent peak current traces and hence can survive differential power analysis (DPA) attacks, resulting in improved circuit security.

Keywords: DSRC, Error control, Hamming code, Adiabatic logic

Introduction

Industrial Internet of Things (IIOT) and cyber physical system technologies contribute majorly to the industry 4.0. Digitalization and intelligent integration are a part of smart industry. Especially, in industry, the short-range communication solutions using digital communication technology should be integrated with no interference to the IIOT. In digital communication, errors are prone to occur due to external factors whenever data transmission takes place from transmitter to receiver. In such a case, the output data is no longer fit with the input data, meaning '0' bit might change to '1' or vice versa. Such errors can grow to be a critical hassle to attain accuracy and system performance. Hence there is a need to improve the reliability of data transmission.[1,2] However, it's far critical to come across and correct the error. The codes such as cyclic, Reed Solomon, Hamming, etc. are available for error control. Hamming code is more efficient and also easy to implement.[2] The DSRC transceiver[3] uses Hamming code for automatic error control which has a lower error rate. Automotive electronic systems must now be secure since they can be attacked through a number of interfaces, direct or indirect physical access, and wireless access channels. Basic Safety Messages (BSM) carry critical information for safety applications including Vehicle-to-Vehicle (V2V) communications.[4–5] Through those various interfaces, it is critical to compromise an Automotive Electronic Control Unit (ECU). ECU-enabled applications include forward collision avoidance, left turn assist and lane change warning among others.[6] Safety, congestion avoidance and energy efficiency are all important metrics in the DSRC system, in addition to security.

Using FinFET based ECRL adiabatic logic,[7,8] in this paper, an attempt is made to reduce the overhead power of error-controlling codes. In terms of power and delay parameters, the effect of adiabatic logic on error controlling code was evaluated.[9,10] The simulations are done with a Cadence tool and an 18 nm FinFET.

Methodology

DSRC Transceiver

The structure of DSRC transceiver system is given in Fig. 1. In order to achieve an error-free

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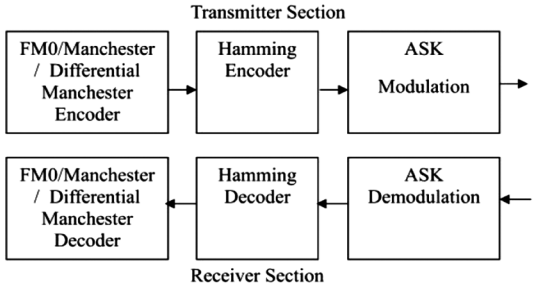

Fig. 1 — DSRC transceiver System

communication, error controlling mechanism must be adopted. As shown in Fig. 1, the data is first encoded at the transmitter side by line encoding techniques like Manchester, FM0, etc.[11] Based on the principles of Hamming code, extra bits are to be added to the encoded data by using Hamming encoder. Finally, the cypher data is transferred over a noisy channel once the encoded data has been modulated. At the receiver side, after demodulating the received cipher data, error control stage, i.e., Hamming decoder detects and corrects the bit in case of any error, giving rise to error-free data output.[12] The applications of the DSRC transceivers includes the intelligent transportation system and various automobiles. The DSRC is the high secure, low latency and high reliability with supporting of interoperability. The received data is very low interference in extreme weather conditions due to its short-range applications.

Hamming Code

Hamming code detects which data bit is in error and also corrects that bit. Addition of parity bits to data word is performed to form the code word.[1–2] The parity bits should be positioned in powers of 2 in the data word. The number of parity bits must be determined based on the length of the data word and is computed as follows.

$$2^P \geq M + P + 1 \quad ...(1)$$

where 'P' indicates the number of parity bits and 'M' the length of data bits. It forms a code word of length (M + P). The type of parity bit to be added is found by exclusive OR operation on the data word. The calculation of parity bits for 8- bit data word is given below.

P1 = EXOR of 3rd, 5th, 7th, 9th, and 11th data bits

P2 = EXOR of 3rd, 6th, 7th, 10th, and 11th data bits

P4 = EXOR of 5th, 6th, 7th, and 12th data bits

P8 =EXOR of 9th, 10th, 11th, and 12th data bits

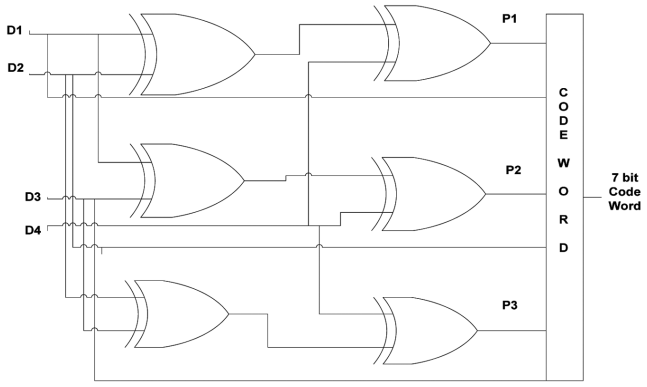

Fig. 2 — A 4-bit Hamming encoder

The code word is generated by using Hamming encoder.[2] A 4-bit Hamming encoder circuit is depicted in Fig. 2. It consists of data word of size 4 bits and parity bit generator of size 3 bits to generate a code word of size 7 bits. In the present work, input data 11000101 of length 8 bits is taken. So, the Hamming encoder requires parity bit generator of size 4 bits. The 8-bit input data is applied to the Hamming encoder circuit. It generates a code word of 12 bits with 8 data bits and 4 parity bits as shown in Table 1. Later, the generated code word is applied to Hamming decoder which detects and corrects the error. It includes checker bit generator of size 3 bits, 3 to 8 decoder and EXOR gates. Since the encoded code word is of 12 bits, the Hamming decoder requires a checker bit generator of size 4 bits, 4 to 16 decoder and EXOR gates. The Hamming decoder locates and corrects the error bit if an error occurs.[2] The checker bits are calculated with EXOR operation on the encoded code word. The checker bits for 12-bit encoded code word are calculated as

C1 = EXOR of P1, D3, D5, D7, D9, and D11 bits

C2 = EXOR of P2, D3, D6, D7, D10, and D11 bits

C3 = EXOR of P4, D5, D6, D7, and D12 bits

C4 = EXOR of P8, D9, D10, D11, and D12 bits

Let us assume that the 10th bit in the encoded code word is corrupted. The actual 10th bit '1' in the encoded data (Table 1) is Changed to '0'. The encoded code word is valid only when no error occurs.

The 12-bit encoded code word shown in Table 1 is applied to Hamming decoder to generate the 4 checker bits C4C3C2C1 by the checker bit generator. In this case it generates 1010 which indicates that the 10th bit received has error. The corrupted bit is corrected by enabling the EXOR gate connected to 4-to-16 decoder.

Table 1 — Encoded code word, received code word with single bit error, and no error

Position of bits	1	2	3	4	5	6	7	8	9	10	11	12
Parity and data bits	P_1	P_2	D_3	P_4	D_5	D_6	D_7	P_8	D_9	D_{10}	D_{11}	D_{12}
Encoded code word	0	0	1	0	1	0	0	0	0	1	0	1
Received code word with one bit error (10^{th} bit)	0	0	1	0	1	0	0	0	0	0	0	1
Received code word with no error	0	0	1	0	1	0	0	0	0	1	0	1

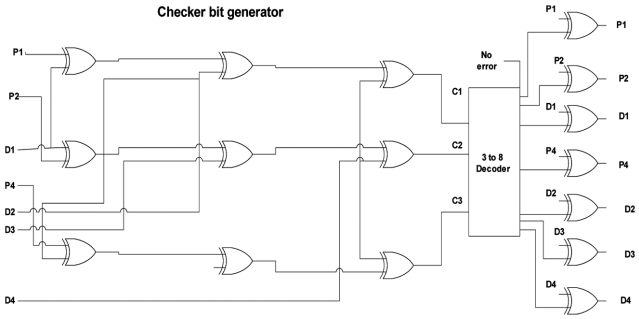

Fig. 3 — Hamming decoder circuit

Efficient Charge Recovery Logic (ECRL)

At the end of the charging process in CMOS logic, the energy received from the supply is decreased to half its initial value. The remaining energy is dissipated during discharge; therefore, the total energy is transformed to heat at the end of one cycle. Using adiabatic logic, the amount of energy dissipated in CMOS circuits can be minimised.[9–10] In adiabatic logic, the charge transfer occurs without generating heat. Instead of using DC supply voltage, a power clock is employed to reduce power dissipation. One of the adiabatic logic families used for power reduction is Efficient Charge Recovery Logic (ECRL).[12]

The ECRL has a very simple structure and comprises of two PMOS transistors which act as pull-up transistors and NMOS transistors as pull-down transistors.[12] The number of NMOS transistors in the pull-down network depends on the number of inputs. The NMOS transistors implement the actual logic. It consists of two complementary outputs. ECRL performs simultaneous pre-charge and evaluation. By making its discharge circuit as symmetric, the ECRL circuit can be effective against Differential Power Analysis (DPA) attacks.[13–15] The ECRL buffer/inverter is shown in Fig. 3.

The two PMOS transistors P1 and P2 of pull-up network are cross-coupled. In Fig. 4 shown, pclk is the power supply, in, inb and out, outb are the true and complementary input and output signals, respectively. Fig. 5 and Fig. 6 respectively shows the ECRL NAND/AND and XNOR/XOR gates.[12]

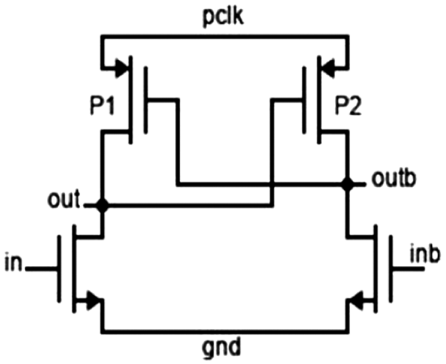

Fig. 4 — ECRL buffer/ inverter

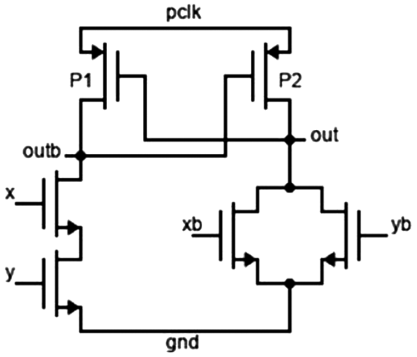

Fig. 5 — ECRL NAND/AND gate

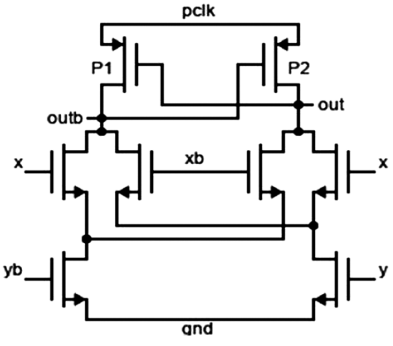

Fig. 6 — ECRL XNOR/XOR gate

FinFET Structure

FinFET is simply called as a 3D transistor. At the nanoscale technology, fin type field-effect transistors (FinFETs) are alternative for bulk CMOS. These are double-gate devices. The multi-gate structure of FinFET allows the device to work in Shorted Gate (SG) and Independent Gate (IG) modes. In SG mode,

the two gates of a FinFET device are shorted in order to achieve higher performance.[7] In IG mode, the two gates can be controlled independently to achieve lower leakage or less transistor count.[8] The IG mode offers more design flexibility. FinFET addresses the challenges posed by continued scaling. The structure of FinFET in both the modes with fin height H_{fin} and silicon thickness t_{si} is shown in Fig. 7.

Simulation Results and Discussion

All the designs of Hamming codec are simulated in Cadence tool. The simulation waveform of parity bit generator is shown in Fig. 8. The parity bits P1P2P4P8 generated are 0000. As the data bits taken are 11000101, the code word obtained is P1P2D3P4D4D5D6D7P8D9D10D11D12 which is 001010000101. Assuming that the tenth bit is corrupted, the code word received is 001010000001. At the transmitter side the tenth bit in the code word is '1', but at the receiver side the tenth bit received is '0'. This position of corrupted bit is obtained by the checker bit generator. The simulation waveform of checker bit generator, comprising of checker bits C8C4C2C1 and 1010(10) is shown in Fig. 9. It indicates that the tenth bit received is in error. This bit is corrected by EXOR gates which are connected to the output of 4 to 6 decoder. The simulation results of decoder are shown in Fig. 10.

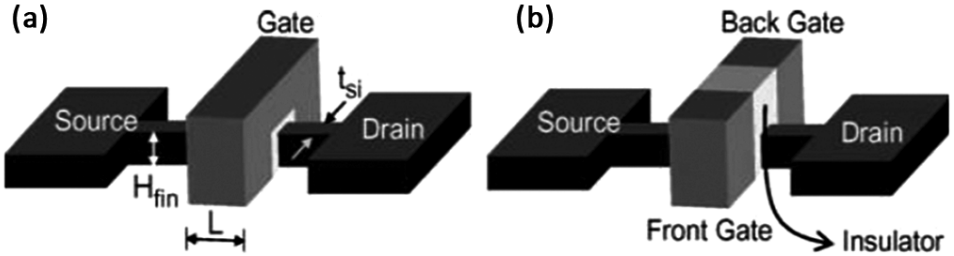

Fig. 7 — FinFET structure (a) shorted gate and (b) independent gate

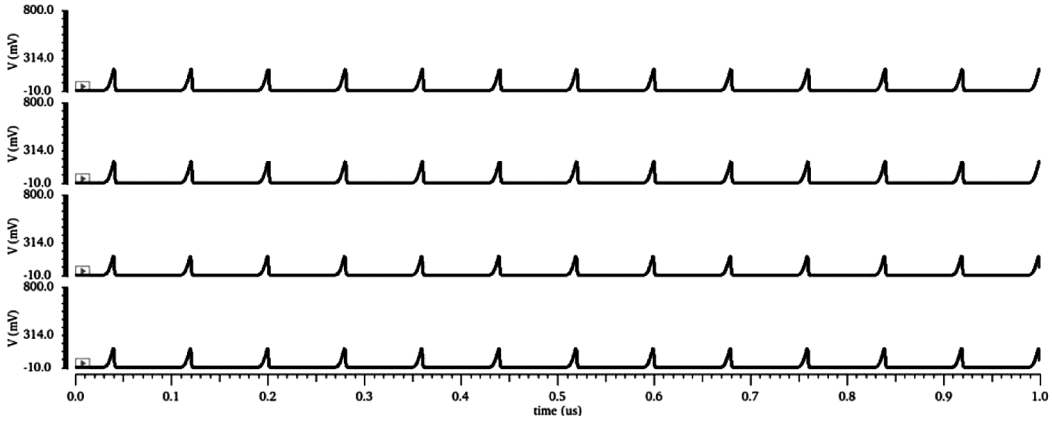

Fig. 8 — Simulation results of parity bit generator P1P2P4P8 (0000)

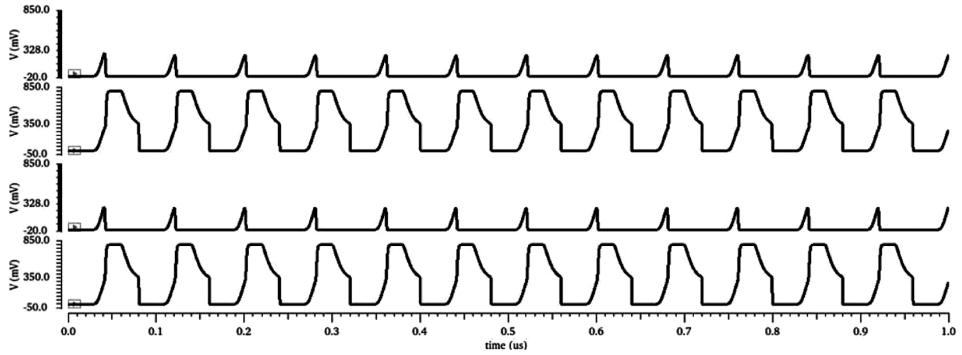

Fig. 9 — Simulation results of checker bit generator C8C4C2C1 (1010)

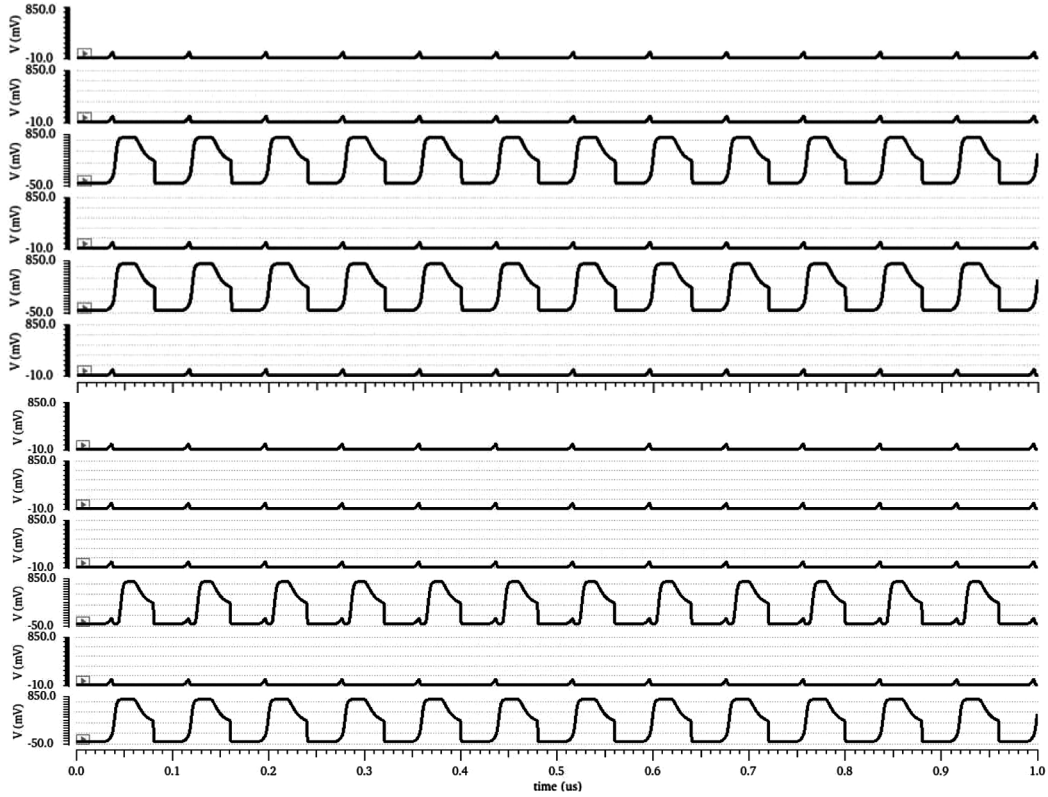

Fig. 10 — Simulation results of hamming decoder (001010000101)

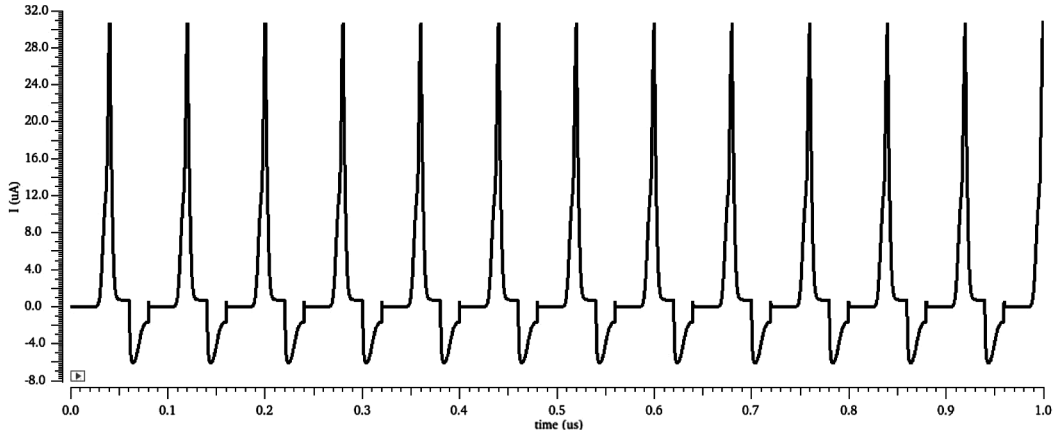

Fig. 11 — Peak current traces of hamming encoder

The code word received is 001010000101 with tenth bit corrected.

The peak current traces of Hamming encoder, hamming decoder and hamming codec are given in Figs 11, 12 & 13 respectively. The peak currents observed for these circuits are 31.5 μA, 135 μA, and 168 μA respectively. The structure given ensures a uniform peak current irrespective of data bits. As a result, the hacker's chances of predicting the encoded data in cyber security hardware is less. The proposed ECRL based adiabatic Hamming codec is highly resistant to differential power analysis attacks.

In Table 2 the comparison of performance characteristics of adiabatic Hamming codec with the reported values are presented.[2] Power savings of the order of 99.49% over CMOS and 99.41% over pass transistor implementation are achieved with the adiabatic logic codec.[2] Adiabatic Hamming codec exhibits 86.13% and 62.38% Power Delay Product (PDP) efficiency compared to CMOS and Pass

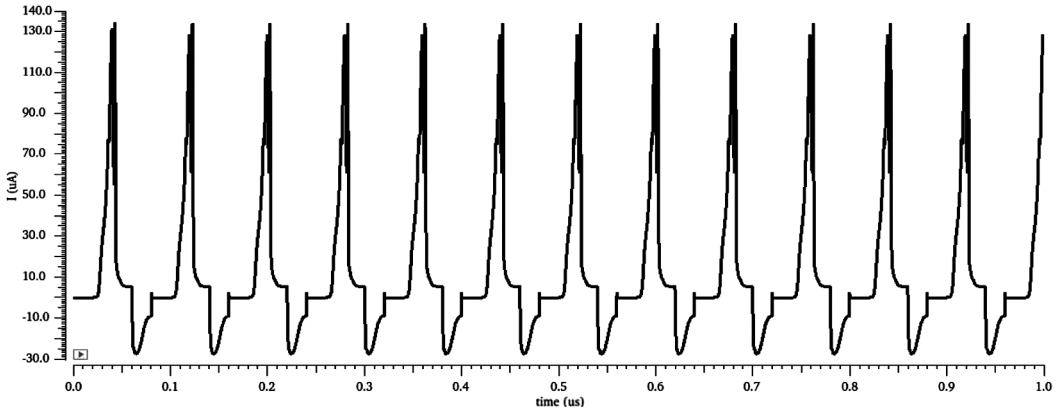

Fig. 12 — Peak current traces of hamming decoder

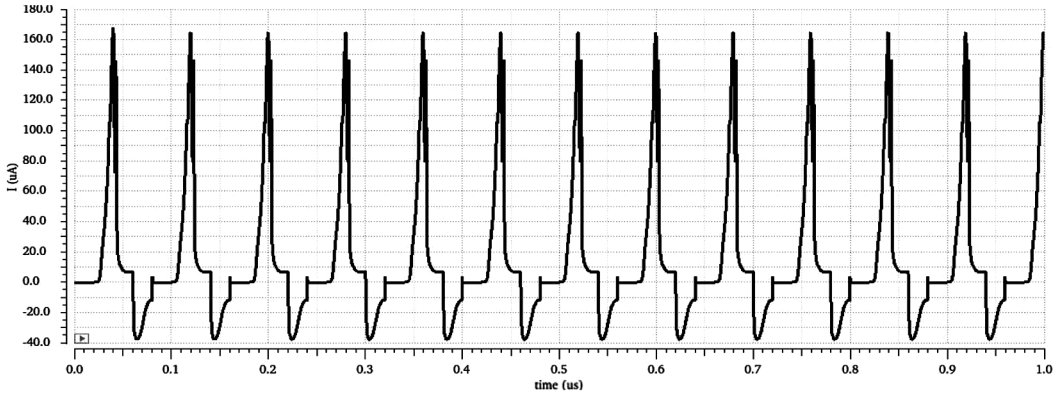

Fig. 13 — Peak current traces of hamming CODEC

Table 2 — Performance characteristics of Hamming encoder, decoder, and codec

Parameter		Chennakesavulu *et al*. [2]		This work
Technology	Scheme	65 nm		18 nm
Device		CMOS	Pass transistor	FinFET
Power(μw)	Hamming encoder	95	82	0.48
	Hamming decoder	393	197	3.44
	Hamming codec	488	279	3.92
Delay(ns)	Hamming encoder	0.081	0.024	1.59
	Hamming decoder	0.164	0.134	2.64
	Hamming codec	0.245	0.158	4.23
PDP (fJ)	Hamming encoder	7.695	1.968	0.766
	Hamming decoder	64.452	26.398	9.081
	Hamming codec	119.56	44.082	16.58

transistor logic. In terms of power and PDP, the adiabatic Hamming codec outperforms CMOS and Pass transistor logic.

Conclusions

Hamming codec for DSRC applications is designed using FinFET based ECRL. The power consumption of the circuit is found to be very small as compared to CMOS and pass transistor implementations. Furthermore, the developed Hamming codec has a similar peak supply current trace, enhancing its resistance to Differential Power Analysis (DPA) attacks and making it ideal for a secure DSRC system. The proposed logic saves the 99.49% of the power comparing with the CMOS and 99.41% power with the over pass transistor implementations using the adiabatic logic codec. Adiabatic Hamming codec exhibits 86.13% and 62.38% PDP efficiency compared to CMOS and Pass transistor logic. The performance of the logic is best suitable of industry related devices.

References

1 Davide B, Luca B & Giovanni D M, Error control schemes for on-chip communication links: The energy–reliability tradeoff, *IEEE Trans Comput Aided Des Integr Circuits Syst*, **24 (6)** (2005) 818–831.

2 Chennakesavulu M, Jayachandra Prasad T & Sumalatha V, Improved performance of error controlling codes using pass transistor logic, *Int J Circuits Syst Signal Process*, **37 (1)** (2017) 1145–1161. https://doi.org/10.1007/s00034-017-0596-4

3 Dhanya V & Martin R, An efficient computerized error control transceiver system for DSRC applications, *ICSPC, (2017)* 112–116. https://doi.org/10.1109/CSPC.2017.8305819.

4 Lin C W & Vincentelli A S, *Security-Aware Design for Cyber-Physical Systems: A Platform Based Approach* (Springer Cham) 2017, 1–99. https://doi.org/10.1007/978-3-319-51328-7.

5 Xinzhou W, Sundar S, Guha R, Robert G W, Junyi Li, Kevin W L, Bucceri A & Zhang T, Vehicular communications using DSRC: Challenges, enhancements and evolution, *IEEE J Sel Areas Commun,* **31 (9)** (2013) 399–408.

6 Kenney J B, Dedicated short-range communications (DSRC) standards in the United States, *Proc IEEE*, **99(7)** (2011) 1162–1182.

7 Muttreja A, Agarwal N, & Jha N K, CMOS logic design with independent-gate FinFETs, IEEE *25th Int Conf on Comput Design* (IEEE) 2007, 560–567.

8 Sherif A T & Volkan K, Low-power and compact sequential circuits with independent-gate FinFETs, *IEEE Trans Electron Devices,* **55(1)** (2008), 60–70. https://doi.org/10.1109/TED.2007.911039.

9 Teichmann P, Adiabatic logic, *Springer Ser Adv Microelectron,* (2012) 5–22, https://doi.org/10.1007/978-94-007-2345-0_2.

10 Athas W C, Sevensson L J, Koller J G, Tzartzains N & Chou E Y C, Low-power digital systems based on adiabatic switching principles, *IEEE Trans VLSI Syst*, **2(4)** (1994) 398–407. https://doi.org/10.1109/92.335009.

11 Lee Y H & Pan C W, Fully reused VLSI architecture of FM0/Manchester encoding using the SOLS technique for DSRC applications, *IEEE Trans Very Large Scale Integr VLSI Syst*, **23(1)** (2015) 18–29. https://doi.org/10.1109/TVLSI.2014.2299532

12 Moon Y & Jeong D K, An efficient charge recovery logic circuit, *IEEE J Solid-State Circuits*, **31(4)** (1996) 514–522, https://doi.org/10.1109/4.499727

13 Thapliyal H, Varun T S S & Kumar S D, Adiabatic computing based low-power and DPA-resistant lightweight cryptography for IoT devices*, In 2017 IEEE Computer Society Annual Symposium on VLSI (ISVLSI)* (IEEE) 2017, 621–626. https://doi.org/10.1109/ISVLSI.2017.115

14 Raghav H S, Bartlett V A & Kale I, A novel power analysis attack resilient adiabatic logic without charge sharing, *Euro Conf on Circuit Theory and Design (ECCTD) (IEEE)* 2017, 1–4. https://doi.org/10.1109/ECCTD.2017.8093262.

15 Kumar S D, Himanshu T, Azhar Md & Kalyan S P, Design exploration of a symmetric pass gate adiabatic logic for energy efficient and secure hardware, *Integration (Amst)*, **58** (2017) 369–377.